

# A novel double-node-upset-resilient radiation-hardened latch

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**Abstract:** To effectively tolerate a double-node upset, a novel double-node-upset-resilient radiation-hardened latch is proposed in 22 nm complementary-metal-oxide-semiconductor technology. Using three interlocked single-node-upset-resilient cells, which are identically mainly constructed from three mutually feeding back 2-input C-elements, the latch achieves double-node-upset-resilience. Using smaller transistor sizes, clock-gating technology, and high-speed transmission-path, the cost of the latch is effectively reduced. Simulation results demonstrate the double-node-upset-resilience of the latch and also show that compared with the up-to-date double-node-upset-resilient latches, the proposed latch reduces the transmission delay by 72.54%, the power dissipation by 33.97%, and the delay-power-area product by 78.57%, while the average cost of the silicon area is only increased by 16.45%.

**Key words:** radiation hardening; circuit reliability; soft error; double-node upset; single-node upset

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The soft error is of transient error resulting from transient faults in digital circuits. In previous device processes, the soft error was mainly considered by researchers for space applications. However, as technology developed, the charge required to change the stage of a circuit node is aggressively decreased due to smaller device capacitances and supply voltages. Consequently, the logic state of a node is becoming more easily disrupted by a transient fault, and the soft errors at terrestrial level are even becoming a concern<sup>[1]</sup>. As a result, it is quite meaningful and valuable to research soft error mitigation, tolerance and even resilience techniques for latches.

In a latch, particle striking may result in the state change of a single-node, which is referred to as a single-node upset (SNU). Recently, many circuit designers have proposed many hardened latches to tolerate an SNU<sup>[2-5]</sup>. However, in nanoscale technology, the de-

crease in node spacing and the decreased critical charge of circuit nodes can allow the single-event charge-collection to affect double nodes, resulting in a double-node-upset (DNU). As a result, charge-sharing induced DNU is becoming a concern, especially, in harsh radioactive environments<sup>[6-7]</sup>.

Accordingly, faced with a DNU, many circuit designers proposed advanced hardened latches to tolerate a DNU<sup>[6,8-13]</sup>. Among these DNU hardened latches, some are DNU partially tolerant<sup>[6,8]</sup> since there is at least one node pair which can be flipped by a DNU resulting in that the latch retains the invalid data; however, the other ones are DNU fully tolerant. In this paper, DNU tolerance is defined as DNU fully tolerance. Note that, DNU fully tolerance does not mean DNU resilience. Among the DNU fully tolerant latches, only some of them are DNU-resilient<sup>[10-13]</sup>. It can be found that these DNU-resilient latches perform with large cost penalties, especially for transmission delay and static plus dynamic power dissipation.

In this paper, a novel DNU-resilient radiation-hardened latch is proposed. An SNU-resilient cell is constructed employing three mutually feeding back C-elements. Then, using three interlocked SNU-resilient cells, the DNU-resilient latch is constructed to tolerate any DNU. Besides, using a high speed transmission path and the clock-gating (CG) technique, the latch reduces considerable transmission delay, power dissipation and delay-power-area product (DPAP) on average compared with the up-to-date DNU-resilient latches. Note that, DNU resilience means that all the nodes can self-recover from any DNU for a latch.

## 1 Existing Hardened Latches

In the existing hardened latches, the C-element is widely used. Fig. 1 shows the circuit structure, symbol and truth table of a 2-input C-element. A C-element behaves as an inverter if its inputs are identical and keeps its previous value if its inputs are different. In Fig. 1(c), Z means high-impedance-state; i. e. a state that keeps the previous correct value for a certain time period.

This section reviews the typical existing examples of SNU and/or DNU hardened latches such as the feedback redundant SEU-tolerant (FERST)<sup>[5]</sup>, low cost and highly reliable (LCHR)<sup>[8]</sup>, double node charge sharing (DNCS)<sup>[9]</sup>, non-temporally hardened latch (NTH-LTCH)<sup>[10]</sup>, double node upset tolerance (DONUT)<sup>[11]</sup>

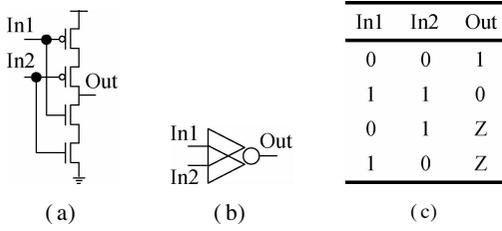
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and so-called DeltaDICE<sup>[12]</sup>.



**Fig. 1** Circuit structure, symbol and truth table of a 2-input C-element. (a) Circuit structure; (b) Symbol; (c) Truth table

The FERST latch is based on dual-modular redundancy, since it has two identical feedback loops connecting to a 2-input C-element at the output stage. Any feedback loop employs a 2-input C-element and an inverter to retain data. Hence, the latch tolerates any SNU. However, if the output of the C-element in any feedback loop is flipped, the latch cannot self-recover, and thus the latch is neither SNU nor DNU-resilient.

The LCHR latch consists of three redundant feedback loops, one of which utilizes a keeper to directly drive its output, and two of which utilize two keepers to drive their output through a C-element at the output stage. Hence, the latch achieves SNU-tolerance but not SNU-resilience. Besides, after a simple investigation, it can be found that the latch cannot tolerate a DNU.

The DNCS latch employs six 2-input C-elements to construct a large soft error interceptive feedback loop to robustly retain data. In the feedback loop, there are many redundant nodes. Among the nodes, by feeding back three critical ones to a 3-input C-element at the output stage, the latch achieves SNU-resilience and DNU-tolerance. However, after a simple investigation, it can be found that the latch cannot self-recover from any DNU.

The NTHLTCH latch is based on triple-modular redundancy. It mainly consists of nine 2-input C-elements, six-TGs and three inverters, and hence triple interlocked feedback loops are constructed. Besides, any feedback loop comprises of three 2-input C-elements, an inverter, and a transmission gate (TG). Hence, the latch achieves SNU-and-DNU-resilience. However, after a simple investigation, it can be found that the latch is not cost-effective.

The DONUT latch is constructed by employing four inter-connected dual-interlocked storage-cells (DICEs), which are self-recoverable from any SNU but not completely self-recoverable from any DNU. Due to having many interlocked redundant hold nodes, the latch achieves DNU-resilience. However, the latch is not cost-effective since no matter what mode of operation, many feedback loops are constructed, resulting in larger power dissipation.

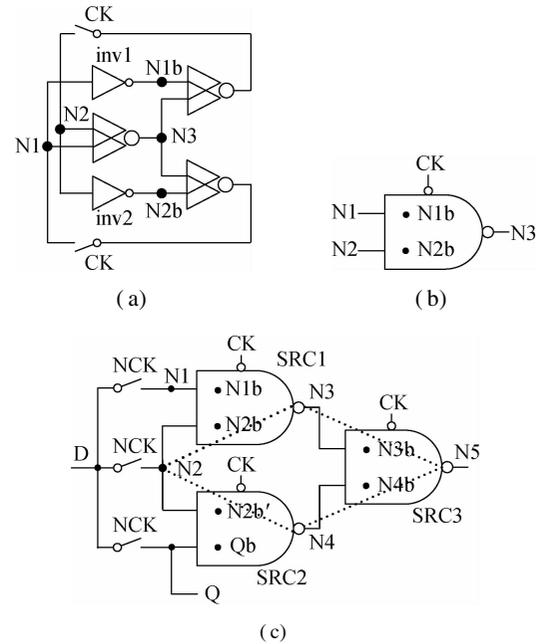
The DeltaDICE latch consists of three inter-connected

DICE cells. The main difference between the DONUT latch and the DeltaDICE latch is the combination way of DICE cells. The DeltaDICE latch can provide many redundant hold nodes to robustly retain data, achieving DNU-resilience. However, similarly to the DONUT latch, the latch is not cost-effective.

## 2 Proposed Hardened DNURH Latch

### 2.1 Circuit structure and behaviour

In Fig. 2, the circuit structure of the proposed double-node-upset-resilient radiation-hardened (DNURH) latch is shown. It can be seen from Fig. 2 (c) that, the latch mainly consists of three TGs (marked as NCK since the gate-terminal of pMOS transistors are connected to NCK) and three inter-connected SNU-resilient cells (SRCs) which are shown in Figs. 2 (a) and (b). Any SRC consists of two TGs (marked as CK since the gate-terminal of pMOS transistors are connected to CK), two inverters and three 2-input C-elements. Note that the SRC shown in Fig. 2(b) comprises of three ports, in which the two ports on the left side are used for positive ones and the right side port is used for the negative one. In the latch, D, Q, CK and NCK are the input, output, system clock and negative system clock, respectively.



**Fig. 2** The proposed HLDUR latch. (a) Structure of the SRC; (b) Symbol of the SRC; (c) Structure of the HLDUR

Primarily, the error free cases are discussed. When CK = 1, the latch works in a transparent mode. The positive ports of SRC1 are driven by D through TGs, and the negative port of SRC1 is driven by N1 and N2 through a 2-input C-element. As for SRC2, it is similar to SRC1. As for SRC3, the positive ports are directly driven by the negative ports of SRC1 and SRC2, and the negative port of is driven by a 2-input C-element. To avoid current

competition on  $Q$  for reducing power and transmission delay, CG technology is used.  $Q$  is prevented from being driven through SRC2 but directly driven by  $D$  through a TG. Since all the positive feedback loops in the SRCs are avoided using the CG technology, the power dissipation can be saved. When  $CK = 0$ , the latch works in a latching mode.  $N1$ ,  $N2$  and  $Q$  are prevented from being driven by  $D$  through TGs, and instead they are feeding back through C-elements in SRC1 and SRC2, respectively. In other words, all the feedback loops in the SRCs are constructed to retain data.

Next, the DNU-resilience is discussed. There are two cases in total: Case I, only a single node is affected in any two SRCs (e. g. node pairs  $\langle N1, N4 \rangle$  and  $\langle N3b, Q \rangle$ ); Case II, double nodes are affected in an SRC (e. g.  $\langle N1, N2b \rangle$  and  $\langle N2, N4 \rangle$ ). As for Case I, since the SRCs are SNU-resilient, the affected nodes can self-recover. Therefore, the latch is DNU-resilient for Case I.

As for Case II, if the affected node pair does not match two ports of an SRC, the internal node like  $N1b$  or  $N2b$  can self-recover via the according positive port through an inverter, and thus the DNU degrades to an SNU. Since the SRCs are SNU-resilient, the latch can self-recover from the degraded SNU. Take  $\langle N1, N2b \rangle$  as an example,  $N2b$  can self-recover by  $N2$  through  $inv2$ , and then the DNU degrades to an SNU and  $N1$  can subsequently self-recover by the correct  $N2b$  and  $N3$  through the C-element. On the other hand, if the affected node pair matches two ports of an SRC, the SRC itself cannot self-recover the correct data. However, there are two other SRCs connecting to this SRC for ensuring enough redundant hold nodes to self-recover. Take  $\langle N2, N4 \rangle$  for an example, if there is no SRC1 and SRC3 connecting to SRC2, the DNU will be retained. Due to the fact that  $N2$  is connected to SRC1,  $N2$  can self-recover through SRC1. As for  $N4$ , the restore back process is similar to that for  $N2$ . Therefore, the latch is DNU-resilient for Case II.

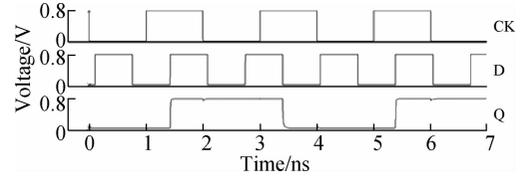
## 2.2 Simulation setup and verification results

The proposed DNURH latch is designed according to the 22 nm complementary-metal-oxide-semiconductor technology and the predictive technology model<sup>[14]</sup> with a supply voltage of 0.8 V and a 2 ns clock period. By means of the Cadence Virtuoso tool, the layout of the latch was drawn. Using the Synopsys HSPICE tool, simulations were performed for SNU-and-DNU-resilience verifications. In the simulations, we perform the fault injections of  $\alpha$  particle induced SNU and DNU and hence a controllable double-exponential-current-source model is used:

$$I_{inj}(t) = \frac{Q}{\tau_\alpha - \tau_\beta} (e^{-t/\tau_\alpha} - e^{-t/\tau_\beta}) \quad (1)$$

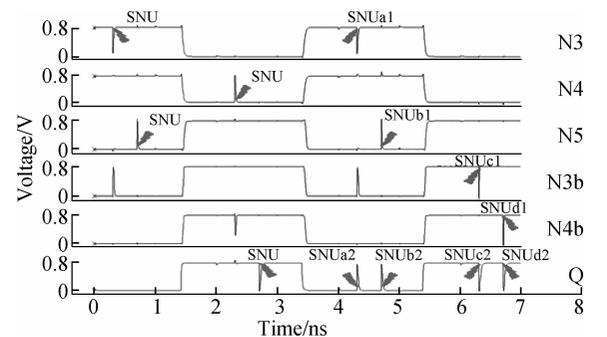
where  $Q$  denotes the injected charge induced by  $\alpha$  particle

striking;  $\tau_\alpha$  and  $\tau_\beta$  are the time constants. In the simulations, we use the large  $Q$  up to 50 fC for a single node.  $\tau_\alpha$  and  $\tau_\beta$  of the current pulse are set to be 3 and 0.1 ps, respectively. Fig. 3 shows the simulation results for the DNURH latch considering an error free case. It can be seen that, the operation of the latch is the same as that of a traditional static D-latch. Note that, the unrelated nodes are omitted in Fig. 3.



**Fig. 3** Simulation results for the DNURH latch considering an error free case

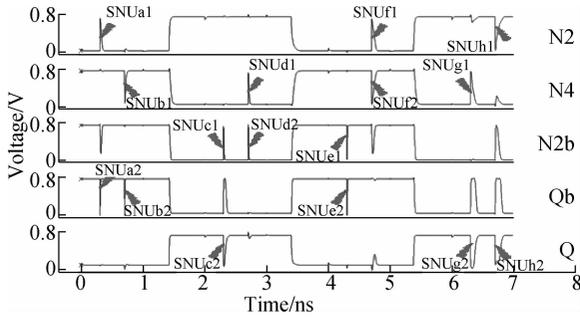
Fig. 4 shows the simulation results for the DNURH latch considering SNUs and Case I for DNUs. If  $N1$  is affected,  $N1b$  will also be affected, which is the same as that for  $N2$  to  $N2b$ , thus the simulations for  $N1b$  and  $N2b$  are omitted. Besides, the SRCs are isomorphic, thus the nodes except for the input and output ports of the SRCs can be omitted for SNU (but cannot be omitted for DNU) simulations in Case I. The latch and the SRCs are all horizontally symmetrical, thus we can only perform the SNU simulation for nodes  $N3$ ,  $N4$ ,  $N5$  and  $Q$  and the DNU simulation for  $\langle N3, Q \rangle$ ,  $\langle N5, Q \rangle$ ,  $\langle N3b, Q \rangle$  and  $\langle N4b, Q \rangle$  in Case I. As shown in Fig. 4, at 0.3, 0.7, 2.3 and 2.7 ns, an SNU is injected on  $N3$ ,  $N5$ ,  $N4$  and  $Q$ , respectively, but the nodes can be restored back from the SNUs. At 4.3, 4.7, 6.3 and 6.7 ns, a DNU is injected on  $\langle N3, Q \rangle$ ,  $\langle N5, Q \rangle$ ,  $\langle N3b, Q \rangle$  and  $\langle N4b, Q \rangle$ , respectively, but the nodes can also be restored back from the DNUs. Note that the simulated DNUs are denoted as  $\langle SNU\lambda1, SNU\lambda2 \rangle$ , in which  $\lambda$  is equal to a to d, respectively.



**Fig. 4** Simulation results for the DNURH latch considering SNUs and Case I for DNUs

Fig. 5 shows the simulation results for the DNURH latch considering Case II and here we take SRC2 for an example. When the affected node pair does not match two of the input or output ports,  $\langle N2, Qb \rangle$ ,  $\langle N4, Qb \rangle$ ,  $\langle Q, N2b' \rangle$ ,  $\langle N4, N2b' \rangle$  and  $\langle Qb, N2b' \rangle$  are simulated for

DNU injections, but when the affected node pair matches two of the input or output ports,  $\langle N4, N2 \rangle$ ,  $\langle Q, N4 \rangle$  and  $\langle N2, Q \rangle$  are simulated for DNU injections. As shown in Fig. 5, at 0.3, 0.7, 2.3, 2.7 and 4.3 ns, a DNU is injected on  $\langle N2, Qb \rangle$ ,  $\langle N4, Qb \rangle$ ,  $\langle Q, N2b' \rangle$ ,  $\langle N4, N2b' \rangle$  and  $\langle Qb, N2b' \rangle$ , respectively, but the node pairs can self-recover. At 4.7, 6.3 and 6.7 ns, a DNU is injected on  $\langle N4, N2 \rangle$ ,  $\langle Q, N4 \rangle$  and  $\langle N2, Q \rangle$ , respectively, but the node pairs can also self-recover. Note that the injected DNUs are denoted as  $\langle SNU\lambda 1, SNU\lambda 2 \rangle$ , in which  $\lambda$  is equal to a to h, respectively. From the above simulations, it can be seen that the DNURH latch is both SNU and DNU resilient.



**Fig. 5** Simulation results for the DNURH latch considering Case II for DNUs

### 3 Latch Comparison and Evaluation

To quantitatively evaluate overheads of the proposed DNURH latch and make a comparison with the existing latches, we similarly performed the simulations for the latches mentioned in Section 1 (FERST<sup>[5]</sup>, LCHR<sup>[8]</sup>, DNCS<sup>[9]</sup>, NTHLTCH<sup>[10]</sup>, DONUT<sup>[11]</sup> and DeltaDICE<sup>[12]</sup>) using the same technology. The transistor sizes of the latches are optimized to reduce overheads, especially, on the silicon area. Here, we take the optimized transistor sizes of the C-elements for an example. The  $W/L$  of the PMOS transistor is 90/22 nm while the  $W/L$  of the NMOS transistor is 28/22 nm. Tab. 1 shows the comparison results of the hardened latches.

**Tab. 1** Comparison results of hardened latches

Latch	Delay/ ps	Power/ $\mu$ W	Area/ USTs	DPAP/ $10^3$
FERST <sup>[5]</sup>	45.71	1.13	95.7	4.94
LCHR <sup>[8]</sup>	61.55	1.04	87.5	5.60
DNCS <sup>[9]</sup>	55.40	2.19	140.2	17.01
NTHLTCH <sup>[10]</sup>	10.76	1.98	139.7	2.98
DONUT <sup>[11]</sup>	18.26	2.18	150.2	5.98
DeltaDICE <sup>[12]</sup>	16.01	2.12	156.8	5.32
Proposed	3.92	1.38	173.0	0.93

In Tab. 1, the data in the first column denote the latch names; the data in the second to the fifth columns denote the D-to-Q transmission delay, the average of static plus dynamic power dissipation, silicon area, and delay-pow-

er-area product (DPAP)<sup>[13]</sup>, respectively. Similarly, the silicon area is measured with equivalent unit size transistors (USTs)<sup>[9, 13]</sup>, and the DPAP metric was calculated by multiplying the delay, power, and silicon area. It can be found that, a smaller DPAP is better.

It can be seen from Tab. 1, to achieve SNU and DNU resilience of the proposed latch, more silicon area has to be used compared with the other hardened latches. The proposed latch has the smallest transmission delay and DPAP due to the use of a direct transmission path from D to Q as well as the CG technology. Compared with the NTHLTCH, DONUT and DeltaDICE latches which are SNU-and-DNU-resilient, the proposed latch has the smallest transmission delay, power dissipation, and the DPAP, which validates the cost effectiveness of the proposed latch except for the silicon area overhead.

In a quantitative point of view, it can be found from Tab. 1 that compared with the up-to-date DNU-resilient latches, the proposed latch reduces transmission delay by 72.54%, power dissipation by 33.97% and DPAP by 78.57% with the cost of only 16.45% silicon area increase on average. Note that, the percentage data for delay is calculated as

$$\text{Percentage}_{\text{Delay}} = \frac{\text{Delay}_{\text{Compared}} - \text{Delay}_{\text{Proposed}}}{\text{Delay}_{\text{Compared}}} \quad (2)$$

Hence, the percentage data for power dissipation, silicon area, and DPAP were calculated. It can be found that although the same type latches can be highly reliably operated, they have larger cost penalties, especially, for transmission delay, power dissipation and DPAP. In summary, the proposed latch can be highly robustly operated and has lower overheads.

### 4 Conclusion

As technology scaling, particle-striking induced SNU and DNU in latches are becoming serious. This paper proposed a novel DNU-resilient radiation-hardened latch in 22 nm complementary-metal-oxide-semiconductor technology. The latch mainly comprises of three single-node-upset-resilient cells to construct many redundant nodes to achieve DNU-resilience. Simulation results demonstrate the DNU-resilience of the latch and also show that the latch has lower costs for transmission delay, power dissipation and DPAP on average compared with the up-to-date DNU-resilient latches.

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## 一种新颖的双节点翻转自恢复的抗辐射加固锁存器

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**摘要:** 为了有效容忍双节点翻转, 提出了一种新颖的 22 nm 互补金属氧化物半导体工艺下双节点翻转自恢复的抗辐射加固锁存器. 使用 3 个互锁的单节点翻转自恢复单元, 并且每个单节点翻转自恢复单元均主要由 3 个互相反馈的二输入 C 单元构成, 该锁存器达到了双节点翻转自恢复性. 使用较小的晶体管尺寸、时钟门控技术和高速传输路径, 有效节省了锁存器的开销. 实验结果验证了该锁存器的双节点翻转自恢复性, 并且与最新的双节点翻转自恢复锁存器相比, 该锁存器平均节省了 72.54% 的传输延迟、33.97% 的功耗和 78.57% 的延迟-功耗-面积复合开销, 而平均的面积开销仅增加了 16.54%.

**关键词:** 抗辐射加固; 电路可靠性; 软错误; 双节点翻转; 单节点翻转

**中图分类号:** TN492