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Influence of the finite size effect of Si(001)/SiO_2 interface on the gate leakage current in nano-scale transistors

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Abstract: With the device size gradually approaching the physical limit, the small changes of the Si(001)/SiO_2 interface in silicon-based devices may have a great impact on the device characteristics. Based on this, the bridge-oxygen model is used to construct the interface of different sizes, and the finite size effect of the interface between fine electronic structure silicon and silicon dioxide is studied. Then, the influence of the finite size effect on the electrical properties of nanotransistors is calculated by using the first principle. Theoretical calculation results demonstrate that the bond length of Si-Si and Si-O shows a saturate tendency when the size increases, while the absorption capacity of visible light and the barrier of the interface increase with the decrease of size. Finally, the results of two tunneling current models show that the finite size effect of Si(001)/SiO_2 interface can lead to a larger change in the gate leakage current of nano-scale devices, and the transition region and image potential, which play an important role in the calculation of interface characteristics of large-scale devices, show different sensitivities to the finite size effect. Therefore, the finite size effect of the interface on the gate leakage current cannot be ignored in nano-scale devices.

Key words: finite size effect; tunneling current; nano-scale transistor

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With the development of technology, the demand of improved performance in the semiconductor transistor has required reducing the device's dimension in recent years, which follows a well-known scaling law known as "Moore's law". The size of the device is further reduced to its physical limit, and the research of small size effect is essential[1-2]. The dominance of Si in microelectronics is largely based on the high quality of the interface between Si and its native oxide SiO_2[3]. Many studies have been devoted to replacing SiO_2 with high-k gate dielectrics. However, in the case of high-k gate dielectrics, very thin SiO_2 is unavoidable[4-5]. Si- and SiO_2-based systems also have the advantage of low cost as well as dealing with abundant, nontoxic, stable and durable materials. Therefore, many experiments and theoretical verifications on Si/SiO_2 interface have been carried out[6-12]. However, the precise bonding information remains controversial[12-15].

So far, there has been much research about the Si/SiO_2 interface structure and electrical properties, and many models have been built[16-18], but these studies mainly focus on using the first principle or other means[19-21] to explore the physical and chemical properties of the interface itself, the impact of the defects or doping on the interface. For example, Wen et al.[22] have used ReaxFF molecular dynamics (MD) simulations to investigate the atomic mechanism of tribo-chemical wear of silicon at the Si/SiO_2 interface; Ono et al.[23] calculated the electronic structure and dielectric properties of interface; Kovačević et al.[11] researched the structure, defects and the stress on the Si/SiO_2, and so on[24-26]. However, the research on the properties of transistor is scarce, and the finite size effect is seldom considered in transistor analysis[27-31]. In this paper, we study the influence of the Si/SiO_2 interface on the characteristics of ultra-thin gate transistor considering the finite size effect. The results will provide a theoretical basis for the application of nano-scale silicon based transistor.

1 First Principle Method

The interface model used in this paper is the bridge-oxygen model (BOM), which is first put forward by Herman et al[32]. It is the simplest and most suitable model for electronic structure calculation[33-36]. This model consists of two layers of Si(see Fig. 1(a)) and two layers of idealized β-cristobalite SiO_2(see Fig. 1(b)). The experi-

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ment lattice constants are 0.543 and 0.716 nm for Si and SiO_2, respectively. The lattice mismatch rate is 32%. The mismatch can be reduced to less than 7% by rotating SiO_2 by an angle of $\pi/4$, as shown in Fig. 1(c). The BOM interface dangling bonds are saturated by adding an oxygen atom to bridge the two Si bonds. Here, the Si-O-Si angle is 144° and the length of Si-O bonds is 0.202 nm. The resulting unit cell has 72 atoms (47 Si and 25 O atoms) and dimensions of 0.5431 nm in the *X*-*Y* plane and 2.5181 nm in the *Z* (growth) direction. To ensure the independence of the interface, a 0.5 nm vacuum layer is added. Finally, the interface structure is obtained in Fig. 1(d). No cell optimization of the model has been carried out.

In order to study the characteristics of the interface in nano-scale transistor considering the finite size effect, six structures with different sizes are constructed, as shown in Fig. 2.

The geometrical optimization and energy calculations are performed using the CASTEP (Cambridge serial total energy package) program[37], which employs the plane pseudopotential method to calculate the total energy within the framework of the Kohn-Sham DFT. The PBE (Perdew, Burke, Ernzerh) formulation of the generalized gradient approximation (GGA) is always used to describe exchange correlation energy[38]. The Vanderbilt ultra-soft pseudo potential is used, which allows numerically converged calculations at relatively low kinetic energy cutoffs of the plane wave basis. The Broyden, Fletcher, Goldfarb and Shanno (BFGS) algorithm is applied to optimize the model structures. The convergence criteria for the self-consistent field (SCF) energy and the displacement are set to be 2.0×10^{-6} eV/atom and 2×10^{-4} nm. $2 \times 5 \times 1$ k-point meshes are taken in the Brillouin zone, and the ground state energy is calculated with the Pulay density mixed method under the following conditions: The precision is 1.0×10^{-5} eV/atom, and the cutoff energy of the plane wave is 340 eV.

Using the DFT theory, the effect of dimensional changes on the characteristics has been studied. Jie et al.[39] used CASTEP to study the influence of GaSe layer variation on optical properties. Niedfeldt et al.[40] also reported the influence of different cell sizes.

2 Results and Discussion

2.1 Electronic structure

It has been pointed out that the change of Si layer will affect the properties of silicon-based devices[41]. Therefore, the influence of the varied *w*/*t* on the Si-Si and Si-O bond length in the interface is first calculated.

Fig. 3 shows the average bond length of Si-Si and Si-O. As seen from Fig. 3, the average bond length of Si-Si gradually decreases with the increase in *w*/*t*, and finally tends to be saturated. On the other hand, although the Si-O bond length increases with the increase in *w*/*t*, it also finally tends to be saturated. These results show that the interface structure tends to be stable due to the influence of the surface state and quantum size effect with the increase in *w*/*t*[42]. The relative change of the Si-Si bond length achieved 3.16%, and the Si-O bond length is as high as 4.53%. Such a large change is very important to the nano-scale transistor. From Fig. 3, we conclude that the finite size effect can be ignored when the width is up to 2 nm and above when the oxide thickness is 2.5 nm.

2.2 Optical properties

By analyzing the electronic structure of the interface, it is found that the increase in *w*/*t* will affect the bond length of the Si side. The change of the structure in the Si side will inevitably affect the optical properties of the interface[41]. The dielectric function is the bridge between the microphysical processes of interband transitions and the electronic structure of materials. ω is the independent variable of the complex dielectric function, $\varepsilon(\omega) = \varepsilon_1(\omega) + i\varepsilon_2(\omega)$, $\varepsilon_1(\omega)$ is the real part and $\varepsilon_2(\omega)$ is the imaginary part of the dielectric function. It mainly represents the transition between the occupied and non-occupied states of electrons, and other spectral information can be easily obtained from it. Therefore, the imaginary part of the dielectric function and the other optical parameters are calculated and analyzed.

The changes in the imaginary part of dielectric function under different ratios of *w*/*t* are given in Fig. 4. It can be seen that the absorption peak shifts to the left and the peak value decreases gradually with the increase in *w*/*t*.

Fig. 5 shows the variation of absorption peak with the increase in *w*/*t*. It can be seen that the absorption peak shifts to the left and decreases gradually with the increase in *w*/*t*. It indicates that with the increase in *w*/*t*, the absorption of photon energy in the high-energy region becomes weaker due to the influence of the surface effect and the quantum size effect. By comparing structure a with structure f, the absorption peak has decreased by almost an order of 10^{-1}. This property can be used to control the optical properties of the transistor.

The change of optical properties with ratio *w*/*t* will lead to the change of electronic properties of devices. Therefore, we next investigate the tunneling current of the nano-scale transistor consisting of the Si/SiO_2 interface with different *w*/*t*.

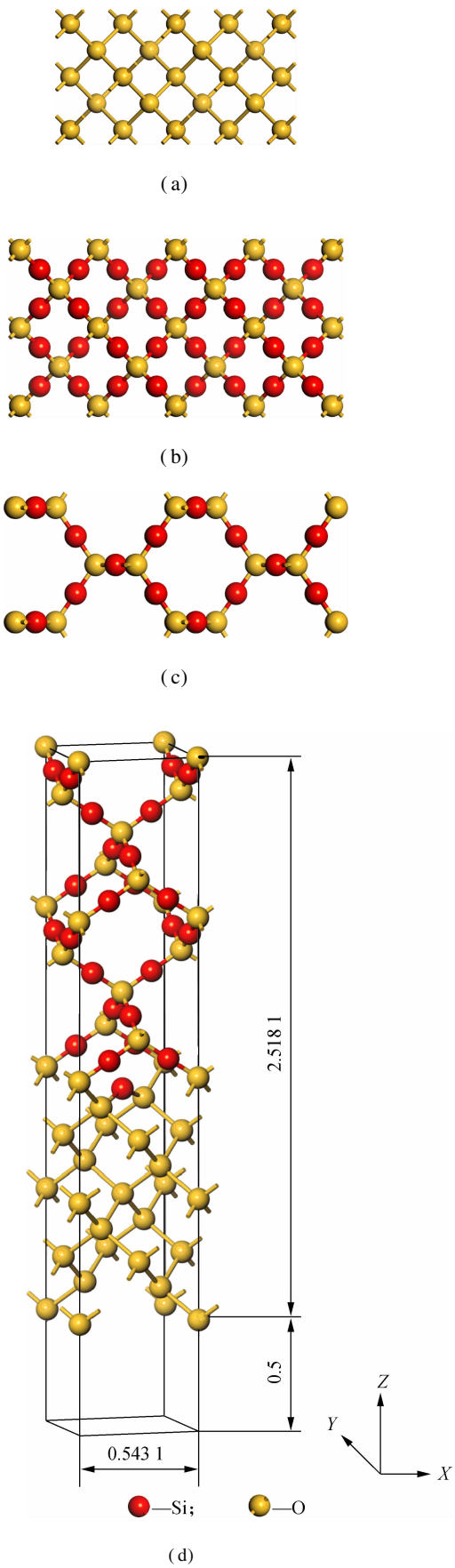


Fig. 1 The BOM model. (a) Two layers of Si; (b) Two layers of idealized β-cristobalite SiO_2; (c) Rotating SiO_2 by an angle of $\pi/4$; (d) The model structure considered in the present study(unit: nm)

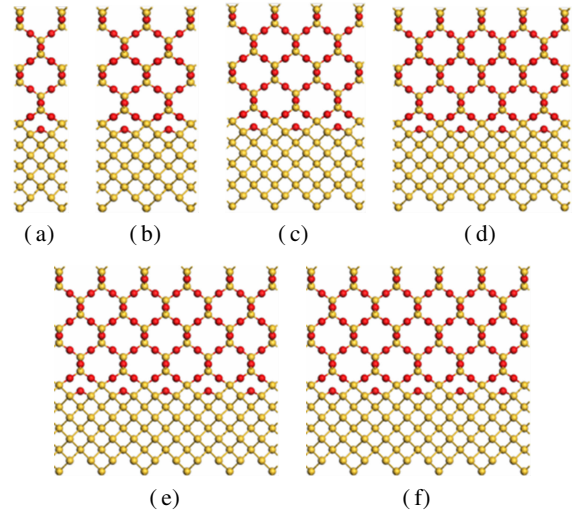


Fig. 2 The structures of six nano-sizes with different ratios of channel width to thickness (w/t). (a) $w/t=1\times5.431/25.181$; (b) $w/t=2\times5.431/25.181$; (c) $w/t=3\times5.431/25.181$; (d) $w/t=4\times5.431/25.181$; (e) $w/t=5\times5.431/25.181$; (f) $w/t=6\times5.431/25.181$

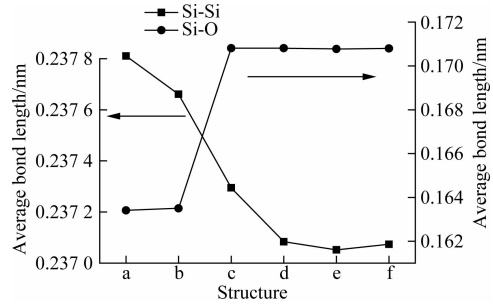


Fig. 3 The average bond length of Si-Si and Si-O for the six nano-sizes

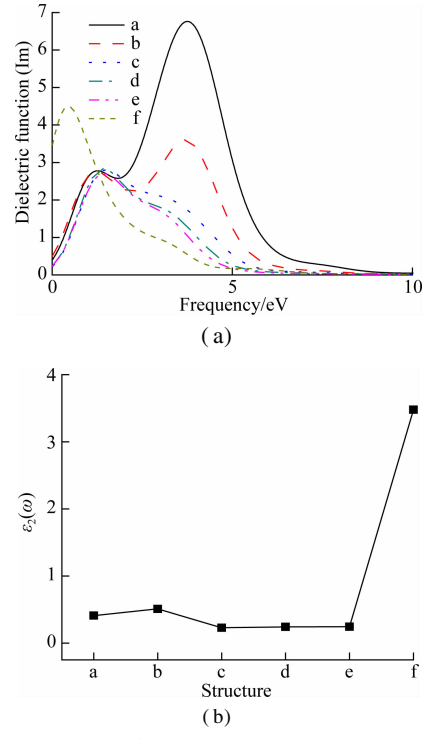


Fig. 4 The dielectric function. (a) The dielectric function in Si/SiO_2 interface for the six nano-sizes; (b) The imaginary part of the dielectric function

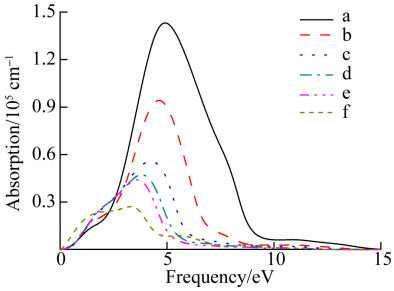


Fig. 5 The size dependence of the absorption in Si/SiO_2 interface

2.3 Energy band profile

2.3.1 Planar microscopic potential via first principles

The valence band profiles are calculated using the average potential method[43]. The electrostatic potential for the super cell is averaged in the *X*-*Y* plane; then, a planar microscopic potential is calculated in the *Z* direction.

$$\overline{V(Z)} = \frac{1}{t}\int_{Z-t/2}^{Z+t/2} V(Z')\,\mathrm{d}Z' \tag{1}$$

At the Si/SiO_2 interface, the band changes continuously from Si to SiO_2 (see Fig. 6). The coordinates Z_1, Z_2 are corresponding to the transition region boundaries and *D* is the width of the transition region. Before the calculation of transistor characteristics, the definition of the transition region is very important. The coordinates in the *Z* direction, corresponding to the band profile changes in a trend away from the averages and vice versa, are set to be the interface region boundaries. For example, the band goes up away from its average at point *A* in Fig. 6, so the coordinate Z_1 corresponding to point *A* can be set to be a boundary for the interface structure. Similarly, the other boundary can be set at Z_2. After measurement, we can obtain the width of the transition region, which is $D = Z_2 - Z_1 = 0.48$ nm. This result is consistent with others reported[16, 26, 36, 44-45] and it is also in agreement with the measured results in the laboratory[46]. By measuring the potential of the structure with six nano-sizes (see Fig. 2) in this paper, *D* remains unchanged at different ratios of *w*/*t*.

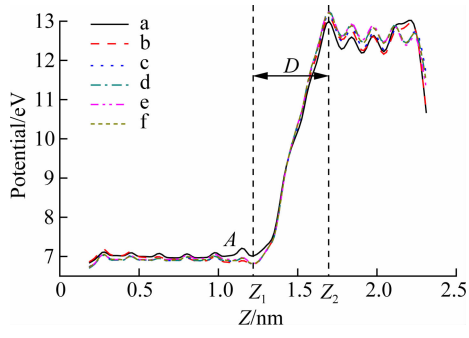


Fig. 6 The planar microscopic potential along the *Z* direction

We can measure the VBM for the six structures with different sizes in Fig. 6, and further obtain the CBM of these structures. The barrier heights are shown in Fig. 7 which are calculated according to Fig. 6. It can be seen clearly that the barrier height curve shows a downward trend, and the trend is getting slower. It is clear that the tunneling current will increase with the increase in *w*/*t* due to the reduction of the barrier height.

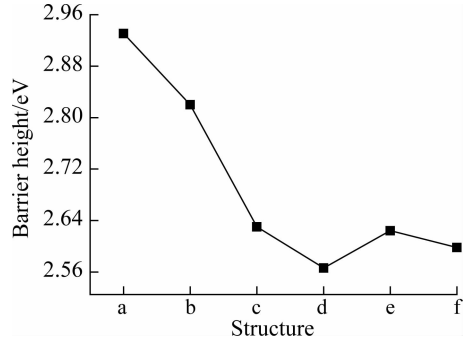


Fig. 7 The barrier height for the six nano-sizes

2.3.2 Gate tunneling current

Ando and Itoh[47] presented a numerical calculation method for gate leakage current with two tunneling conditions:

$$J_{FN} = BE_{ox}^2 \exp\left(-\frac{C}{E_{ox}}\right) \tag{2}$$

$$J_{DT} = \frac{B}{B\left(1-\left(1-\frac{V_{ox}}{\phi}\right)^{1/2}\right)^2}E_{ox}^2 \cdot \exp\left(-\frac{C}{E_{ox}}\times\left(1-\left(1-\frac{V_{ox}}{\phi}\right)^{3/2}\right)\right) \tag{3}$$

where V_{ox} is the voltage added to the barrier layer, and the electric field in the oxide is $E_{ox} = V_{ox}/T_{ox}$. T_{ox} is the oxide thickness. *B* and *C* are given, respectively, by

$$B = \frac{q^3 m}{16\pi^2 \hbar\, m_{ox}^* \phi} \tag{4}$$

$$C = \frac{3(2m_{ox}^*)^{1/2}}{4q\hbar}\phi^{3/2} \tag{5}$$

where *q* is the free electron charge; ϕ is the potential barrier height (eV) at the metal-oxide interface ignoring the effect of the image potential; $\hbar$ is reduced Plank's constant; *m* is the free electron mass; m_{ox}^* is the effective mass of electrons in the conduction band in oxide.

The above classical tunneling current formulae approximately consider the interface region to be abrupt, and do not consider the influence of image potential. However, it can be clearly seen that the potential changes in the interface are not abrupt as shown in Fig. 6. On the other hand, it will reduce the area and the thickness of the barrier due to the existence of the image potential. This will cause an increase in the tunneling current. Furthermore, when the oxide layer becomes ultra-thin and the applied

voltage is below the potential barrier height, the classical FN formula is not applicable[48].

Taking the transition region (width D) into account, the FN tunneling current through a triangular barrier can be rewritten as[49]

$$J_{\text{transtion}} = J_{\text{FN}}\exp\left[\frac{2D\sqrt{2m_{\text{ox}}^{*}\phi_{\text{eff}}}}{3\hbar}\right] = B_1 E_{\text{ox}}^2 \exp\left(-\frac{C}{E_{\text{ox}}}\right) \tag{6}$$

where

$$B_1 = B\exp\left(\frac{2D\sqrt{2m_{\text{ox}}^{*}\phi_{\text{eff}}}}{3\hbar}\right) \tag{7}$$

Taking the effect of barrier lowering induced by image potential into account, the direct tunneling (DT) current can be rewritten as[48]

$$J_{\text{image}} = J_{\text{DT}}\exp\left(\frac{D\sqrt{2m_{\text{ox}}^{*}\phi_{\text{eff}}}}{\hbar}\right) \tag{8}$$

where $\phi_{\text{eff}} = \phi - E_{\text{ox}}$. The transition region width D is calculated according to Fig. 6. The barrier heights without electric field(ϕ) are also given for the six structures in Fig. 7. Other parameters used in this work are $m_{\text{ox}}^{*} = 0.5$ m, $\hbar = h/(2\pi)$, $D = 0.48$ nm.

Using Eq. (6), the FN tunneling current considering the transition region can be obtained in Fig. 8(a). It shows the FN tunneling current under different applied voltages across gate oxide with different ratios of w/t. It can be seen that the tunneling current increases gradually with the increase in the ratio, but the trend of the increase decreases, which is corresponding to the observed electronic structure (see Fig. 3). In Fig. 8(b), the change in the ratio of $J_{\text{trans}}/J_{\text{trans0}}$ as a function of the applied gate voltages is calculated, where J_{trans0} is the FN tunneling current without the finite size effect. The FN tunneling current becomes larger considering the finite size effect than that without considering. The ratio decreases with the increase in the electric field of the oxide layer. When the electric field is 10 MV/cm, the ratio of $J_{\text{trans}}/J_{\text{trans0}}$ is up to 45 for structures with different sizes. However, when the field increases to 20 MV/cm, the ratio is only 4. Clearly, the FN tunneling current will increase due to the finite size effect. The increased amount becomes smaller when the electric field is increased.

Fig. 9(a) shows the change of J_{image}, which is calculated using Eq. (8). It can be seen that the direct tunneling current already exists in the low voltage region which is different from the FN tunneling current. The direct tunneling current will increase with the increase in w/t. We can also see that the currents have an obvious turning point in the high voltage region, and the current increases significantly after the turning point. In an ultra-thin gate transistor, the gate field will increase with the decrease of the gate thickness, which corresponds to the high voltage region in which the direct tunneling current is significantly increased. Through this result, we find that the effect caused by sizes cannot be ignored as the size of the transistor decreases.

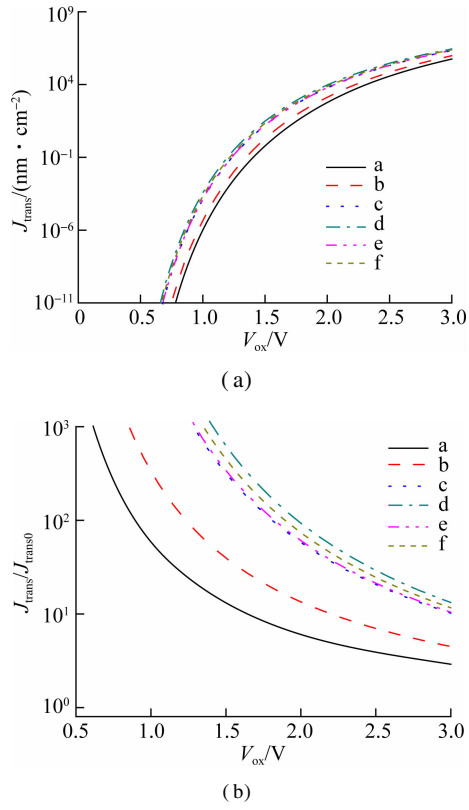


Fig. 8 The FN tunneling current as a function of the applied voltage across gate oxide with different w/t for the six structures ($T_{\text{ox}} = 1.62$ nm). (a) The change of J_{trans}; (b) The change in the ratio of $J_{\text{trans}}/J_{\text{trans0}}$

Fig. 9(b) shows the change in the ratio of $J_{\text{image}}/J_{\text{image0}}$, where J_{image0} is the direct current without the finite size effect. It can be seen that the direct current will increase due to the finite size effect. It also shows that with the increase in gate voltage, there are two turning points in the current curve. When near the FN tunneling area, the influence of the finite size effect is almost saturated and declines. This indicates that the influences of the finite size effect on the direct tunneling and FN tunneling are different. When the electric field is 10 MV/cm, the ratio of $J_{\text{image}}/J_{\text{image0}}$ is only 3 for structures with different sizes. We can conclude that the finite size effect has a greater impact on the FN tunneling current than on the direct tunneling current.

Figs. 10(a) and (b) show the changes in the ratios of $J_{\text{trans}}/J_{\text{FN}}$ and $J_{\text{image}}/J_{\text{DT}}$, where J_{FN} is the tunneling current without the transition region, and J_{DT} is the direct tunneling current without considering the effect of image potential. It can be seen that both the tunneling current will increase with the transition region and image potential. However, the existence of the finite size effect has redu-

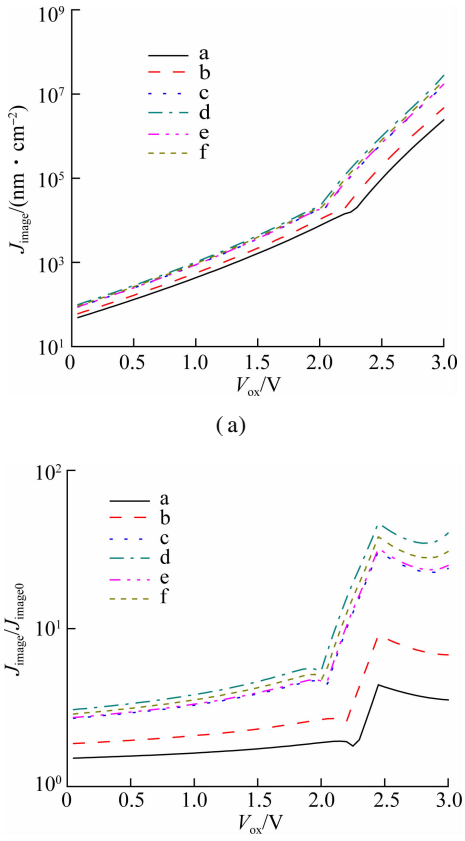


Fig. 9 The direct tunneling current as a function of the applied voltage across gate oxide. (a) The change of J_{image}; (b) The change in the ratio of J_{image}/J_{image0}

ced the influence of the transition region and image potential, and leads to a decrease in the ratio of J_{trans}/J_{FN} and J_{image}/J_{DT}, separately. It also shows that with the increase in gate voltage, both J_{trans}/J_{FN} and J_{image}/J_{DT} will gradually decrease.

Fig. 11(a) shows the change in the ratio of J_{trans}/J_{FN}, in which the currents are calculated under different gate voltages and oxide thicknesses when the barrier height is $\phi = 3.15$ eV. It can be seen that the influence of the transition region on the tunneling current decreases with the increase in the gate voltage under the same oxide thickness. Furthermore, the degree of decline will gradually increase with the decrease of the oxide thickness. The ratio of J_{trans}/J_{FN} decreases from 7.8 to 4.5 with $T_{ox} = 1$ nm when the gate voltage changes from 0 to 3 V. On the other hand, the ratio decreases from 7.8 to 6.8 with $T_{ox} = 3.5$ nm when the gate voltage changes from 0 to 3 V. This is because with the decrease in thickness, the transition region occupies a larger proportion of the whole interface region. Therefore, considering the transition region or not will produce a greater impact on the tunneling current when the oxide thickness is smaller.

Fig. 11(b) shows the change in the ratio of J_{image}/J_{DT} under different gate voltages and oxide thicknesses, separately. Comparing Fig. 11(a) and (b), we find that alth-

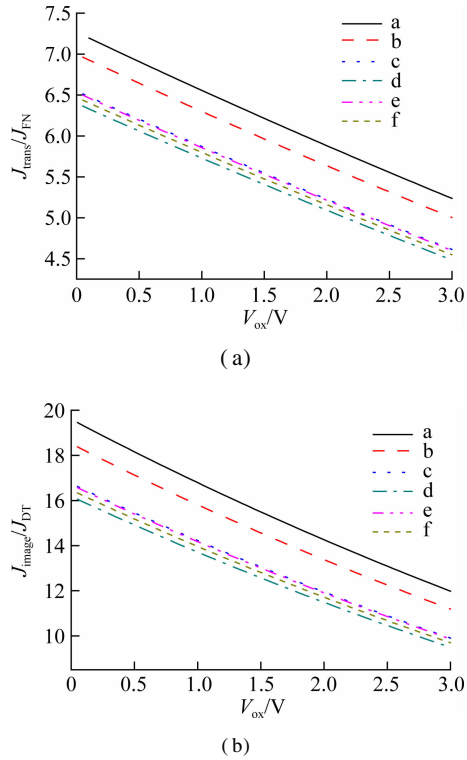


Fig. 10 The tunneling current as a function of the applied voltage across gate oxide. (a) The change in the ratio of J_{trans}/J_{FN}; (b) The change in the ratio of J_{image}/J_{DT}

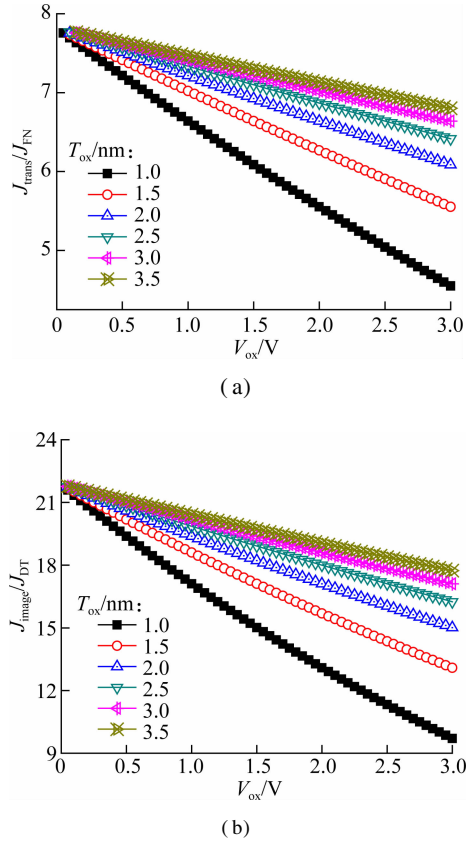
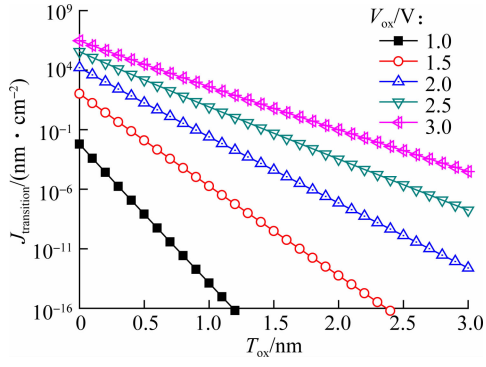


Fig. 11 The tunneling current as a function of the applied voltage across gate oxide with different oxide thickness. (a) The change in the ratio of J_{trans}/J_{FN}; (b) The change in the ratio of J_{image}/J_{DT}

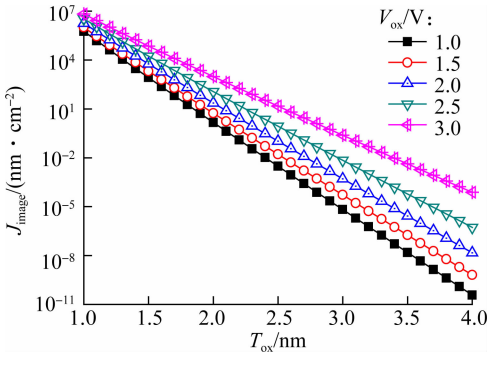
ough the ratio is greater for direct tunneling current than for the FN tunneling current at the same oxide thickness and same gate voltage, the variation trend is similar, which is consistent with the numerical results obtained by Mao et al[48]. J_{image}/J_{DT} decreases with the increase in gate voltage. We also conclude that considering the image potential or not will produce a greater impact on the tunneling current when the oxide thickness is smaller. The ratio of J_{image}/J_{DT} decreases from 21.6 to 9.7 when the gate voltage changes from 0 to 3 V. This ratio is lower than that of FN tuneling which is shown in Fig. 11(a). These results indicate that the direct tunneling current is more dependent on oxide thickness than on the FN tunneling current.

It has been pointed out that the threshold voltage modulation of an MOSFET is affected not only by the channel length of the transistor, but also by its channel width[50]. The conclusions of this paper are consistent with the experimental conclusion that the leakage current becomes larger when the channel width increases[51].

Fig. 12(a) shows the change of FN tunneling current calculated by Eq. (6) with different oxide thicknesses and applied gate voltages. It can be clearly seen that the tunneling current increases with the decrease of oxide thickness when the same gate voltage is applied. The dependence on the thickness of the oxide layers is greater while the gate voltage is smaller. Also, we conclude that under the same oxide thickness, the tunneling current decreases rapidly with the decrease of the gate voltage, and the tunneling current of FN is almost ignorable in the low voltage region (the current ranges from the magnitude of the 10^{-4} to the order of magnitude of 10^{-36}). This is consistent with the conclusion obtained by Yeo et al[52].



(a)



(b)

Fig. 12 The tunneling current as a function of the oxide thickness with different applied voltage across gate oxide($\varphi = 3.15$ eV). (a) The FN tunneling current; (b) The direct tunneling current

Fig. 12(b) shows the variation of the direct tunneling current under different gate voltages and oxide thicknesses, and the barrier reduction effect caused by the image potential is considered. It can be seen that the direct tunneling current reduces with the increase in the oxide thickness when the same gate voltage is applied. When the oxide thickness ranges from 1 to 4 nm, the direct tunneling current is reduced by 14 orders of magnitude when applied voltage is 2 V. The value is 11 when the applied voltage is 3 V. Under the same oxide thickness, the tunneling current increases with the increase in the gate voltage. It is also shown that the direct tunneling current cannot be ignored in a transistor with oxide thickness less than 3 nm.

These results indicate that the FN tunneling current is more dependent on the applied voltage across the gate oxide in the nano-scale transistor. We also conclude that when traditional methods such as increasing oxide thickness or reducing gate voltage are no longer useful for decreasing the leakage current, we can use the finite size effect to achieve this.

3 Conclusions

1) Both the bond length of the Si-Si and Si-O at the interface will be saturated when the interface size increases.

2) The finite size effect must be considered when the interface size is less than 2 nm. It can cause a change in the absorption spectrum of visible light. It implies that the absorption spectrum of visible light can be used as a tool to characterize the interface size.

3) When the device is nanoscale, the barrier height of Si/SiO_2 decreases with the decrease of the interface size.

4) The tunneling current is significantly changed due to the finite size effect. It is well known that the existence of the transition region and image potential will cause a greater tunneling current. However, the increasing ratio will be weakened by the finite size effect.

5) This work can help us to clarify the impact of the finite size effect of the Si/SiO_2 interface on tunneling current in nano-scale transistors. Not only can we better understand the characteristics of the interface, but also help to optimize the parameters of the next generation of nano-transistors in the future.

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硅与二氧化硅界面的有限尺寸效应对纳米晶体管栅漏电流的影响

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摘要:随着器件尺寸逐渐逼近物理极限,硅基器件中硅与二氧化硅界面的微小变化都会对器件特性造成很大的影响,基于此,运用桥氧模型构建了不同尺寸的界面,研究了精细电子结构硅与二氧化硅界面的有限尺寸效应,进而利用第一原理计算了其对纳米晶体管电性能的影响. 理论计算结果表明,硅-硅和硅-氧的键长随尺寸的增大呈饱和趋势,界面对可见光的吸收能力以及界面的势垒则随尺寸的减小逐渐增大. 最后,隧穿电流的研究结果表明,界面的有限尺寸效应对纳米级别器件的栅极漏电流存在很大的调控作用,而且在大尺寸器件界面特性计算中起重要作用的过渡区和镜像电势,对有限尺寸效应表现出了不同的敏感度. 因此,界面的有限尺寸效应对栅极漏电流的影响在纳米级别的器件中已经不可忽略.

关键词:有限尺寸效应;隧穿电流;纳米级晶体管
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