

3D heterogeneous integration of wideband RF chips using silicon-based adapter board technology

Wang Yong^{1,2} Wei Wei² Yang Dong³ Sun Biao²
Zhang Xingwen² Zhang Youming^{4,5} Huang Fengyi^{4,5}

(¹School of Information Science and Engineering, Southeast University, Nanjing 210096, China)

(²Yangzhou Marine Electronic Instrument Institute, Yangzhou 225001, China)

(³Hebei Semiconductor Research Institute, Shijiazhuang 050002, China)

(⁴School of Cyber Science and Engineering, Southeast University, Nanjing 210096, China)

(⁵ Purple Mountain Laboratories, Nanjing 211111, China)

Abstract: An ultra-wideband mixing component cascaded by a mixing multi-function chip and a frequency multiplier multi-function chip was demonstrated and implemented using 3D heterogeneous integration based on the silicon adapter board technology. Four layers of high-resistance silicon substrate stack packaging are implemented based on the wafer-level gold-gold bonding process. Each layer adopts though silicon via (TSV) technology to realize signal interconnection. A core monolithic integrated microwave chip (MMIC) is embedded in the silicon cavity, and the silicon-based filter is integrated with the high-resistance silicon substrate. The interconnect line, cavity and filter of the silicon-based adapter board are designed with AutoCAD, and HFSS is adopted for 3D electromagnetic field simulation. According to the measured results, the radio frequency (RF) of the mixing multi-function chip is 40-44 GHz and its intermediate frequency (IF) can cover the Ku band with a chip size of 10 mm × 11 mm × 1 mm. The multiplier multi-function chip operates at 16-20 GHz. The fundamental suppression is greater than 50 dB and the second harmonic suppression is better than 40 dB with a chip size of 8 mm × 8 mm × 1 mm. The cascaded fully assembled mixing component achieves a spur of better than -50 dBc and a gain of better than 15 dB.

Key words: silicon-based adapter board; frequency mixing; frequency multiplier; multi-function chip

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With the rapid development of electronic information technology, the electronic countermeasure (ECM) will be faced with demanding requirements in terms of sensitivity, wide instantaneous bandwidth, anti-interference ability and portability. Therefore, as the core part of an ECM system, high-performance, miniaturized mixing components have become one of the important research

directions. With the development of bulk silicon micromachining technology, the use of new technologies such as the micro-electro-mechanical system (MEMS) and though silicon via (TSV) to develop miniaturized transceiver systems has become a new option^[1-7]. With the silicon-based adapter board technology, it is possible to integrate passive and active devices (GaAs, CMOS chips, etc.) on a single high-resistance silicon substrate^[8]. Combining SIP, SOP, POP and other 3D integration technologies, the SWP performance of the ECM system will be further maximized^[9-11].

In this paper, using silicon-based adapter board technology, the broadband miniaturized 3D heterogeneous integrated chips covering the Ku frequency band are realized, and the silicon-based interdigital band filter is optimized. Using TSV and wafer-level gold-gold bonding and other 3D integration technology, the integrated design of the microwave chip and passive filter is implemented. Then, a mixing component is assembled by the proposed mixing multi-function chip and frequency multiplier multi-function chip and can better meet the needs of miniaturized applications.

1 Overall Scheme

The block diagram of the broadband mixing component is shown in Fig. 1. The key point of the design is to optimize specifications such as in-band spurs without worsening the noise figure (NF). The quality of the NF depends on the gain of the RF circuit. In other words, a higher front-end circuit gain helps to improve the NF of the mixing component. The spur performance mainly depends on the mixing intermodulation suppression capability and the relative bandwidth of the RF/IF. In order to ensure that the spur after the two conversions does not fall within the signal bandwidth, the design adopts an extremely high frequency local oscillator (LO) mixing scheme and double conversion, in which the frequency of the first conversion LO signal is close to 60 GHz. Meanwhile, to ensure the quality factor of the LO signal, the LO generating circuit uses a frequency multiplier multi-function chip circuit based on a triple frequency multipli-

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Biographies: Wang Yong (1983—), male, Ph. D. candidate; Zhang Youming (corresponding author), male, doctor, associate research fellow, zhangyouming@seu.edu.cn.

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er. This paper mainly focuses on the miniaturized integration of the mixing multi-function chip and frequency multiplier multi-function chip with high performance.

As shown in Fig. 1, the mixing multi-function chip integrates functional circuits such as band-pass filter, mixer, attenuator, amplifier, and adopts double balanced mixing circuits to achieve a general design of the two-stage mixing units, while the frequency multiplier chip

mainly integrates functional circuits such as the frequency tripler, band-pass filter and amplifier to reduce the design difficulty of millimeter wave LO and the risk of electromagnetic leakage of extremely high frequency signals. Both of the multi-function chips use advanced 3D heterogeneous integration technology to achieve miniaturized integration.

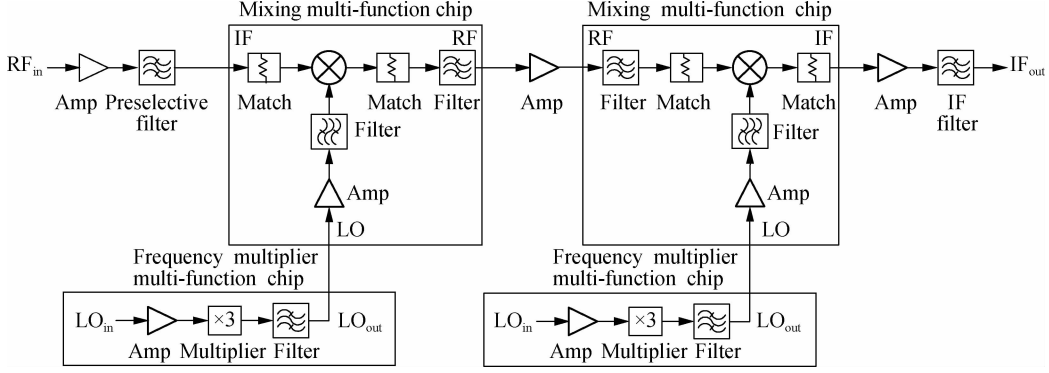


Fig. 1 Block diagram of the broadband mixing component

2 Design of the 3D Heterogeneous Integrated Chips

Aimed at the integration of the above two multi-function chips, this paper proposes a silicon-based 3D stack structure model. As shown in Fig. 2, there are four silicon-based layers. The first layer is the grounding base layer; the core monolithic integrated microwave chip (MMIC) is embedded in the second layer of the silicon cavity; the silicon-based filter is integrated with the high-resistance silicon substrate in the third layer. Each layer adopts TSV technology to realize signal interconnection. Four layers of high-resistance silicon substrate stack packaging are implemented based on the wafer-level gold-gold bonding process.

filtering on the chip. The key problem of the mixing multi-function chip is how to design a suitable filter to complete the high- Q transmission of RF and LO signals.

The filtering function of RF and LO signal is realized by the silicon-based interdigital strip filter structure. The simulation model of the RF silicon-based filter is shown in Fig. 3, and the simulation results are shown in Fig. 4. It can be seen that the filter suppression is greater than 20 dB at 39 and 45 GHz, and the suppression is greater than 70 dB at 34.5 and 49.5 GHz, which meets the basic design requirements.

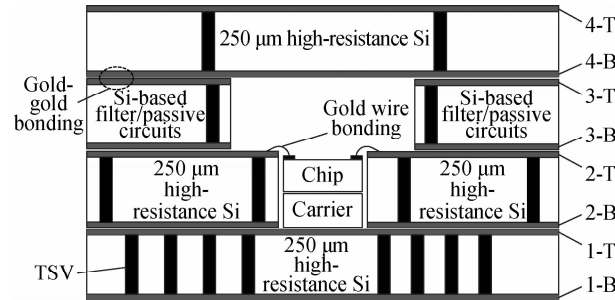


Fig. 2 Model of silicon-based multi-function chip

2.1 Design and simulation of the mixing multi-function chip

The mixing multi-function chip mainly processes frequency conversion on the pre-stage RF signal of the downconverter, and mainly integrates the functions of amplification, frequency conversion, LO and IF signal

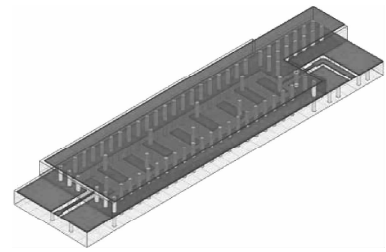


Fig. 3 Simulation model diagram of RF silicon-based filter

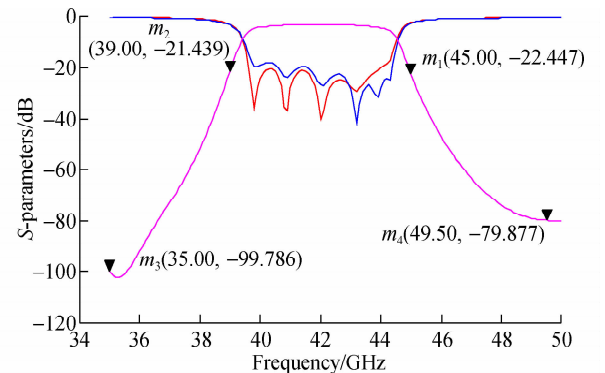


Fig. 4 Simulation results of RF silicon-based filter

Considering the loss and matching performance of microstrip transmission for the 60 GHz LO signal in the packaged chip, a substrate integrated waveguide (SIW) transmission structure that is more suitable for millimeter wave transmission is employed to ensure the quality of RF signal transmission. In addition, in order to facilitate the bonding connection between the internal chip and the microstrip structure, a coplanar waveguide (CPWG) to SIW plane transmission structure is applied, and more dense ground vias are used around the transmission structure to ensure isolation. The transmission structure design and simulation results of CPWG to SIW are shown in Figs. 5 and 6.

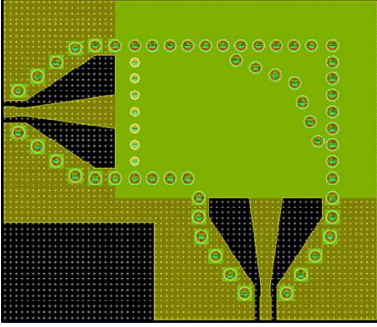


Fig. 5 The transmission structure of CPWG to SIW

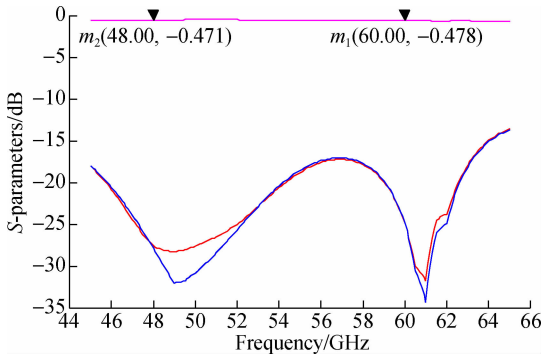


Fig. 6 The simulation results of CPWG to SIW

It can be seen that the 90° transmission structure from CPWG to SIW has a VSWR of less than 1.5, a loss of less than 0.5 dB, and a flatness of less than 0.1 dB in the entire frequency band, which shows excellent performance.

2.2 Design and simulation of frequency multiplier multi-function chip

The frequency multiplier multi-function chip integrates amplifier, attenuator, frequency tripler and filter. In order to reduce the transmission loss of the high frequency millimeter wave signal and solve the electromagnetic compatibility problem of the signal in the frequency conversion component, the frequency multiplier multi-function chip is used to triple the LO signal in the Ku band to obtain the extremely high frequency LO signal required for mixing. According to the mixing spurious index, the

suppression of the fundamental wave ($1/3 \times \text{LO}$) and the second harmonic ($2/3 \times \text{LO}$) of the LO signal must be greater than 90 dBc.

This work is based on a two-stage silicon-based strip-line filter to achieve a high rejection design of the LO filter, and the two-stage filters are placed in different packaged chips (multiplication and mixing multi-function chips) to reduce their mutual influence. The single-stage filter structure is shown in Fig. 7, and the simulation results are shown in Fig. 8. It can be seen that the suppression of the single-stage filter is better than 55 dBc at 40 GHz, and the cascade suppression of the two-stage filter is better than 100 dBc. In addition, the LO frequency of the second-stage mixing of the down-converter described in this paper is set between 48 and 60 GHz. Along with the filtering structure, the same frequency multiplier multi-function chip can be used for the two-stage mixer.

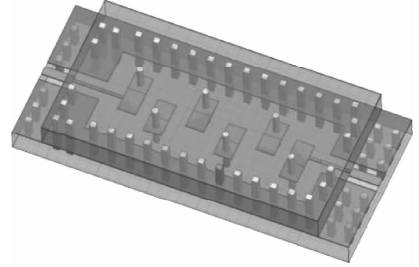


Fig. 7 LO silicon-based filter simulation model diagram

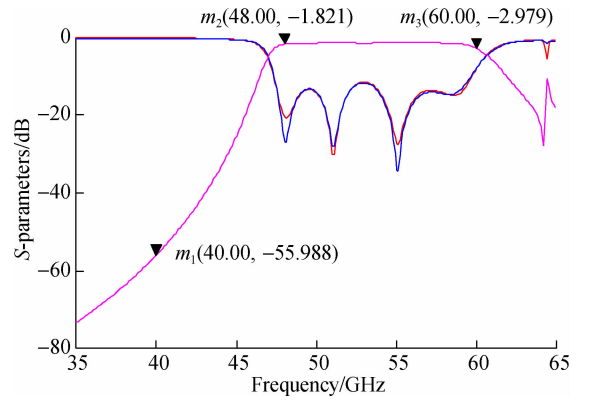


Fig. 8 LO silicon-based filter simulation results

3 Implementation Results

3.1 Test results of the multi-function chips

The cavity and inter-connect line of the silicon-based adapter board are designed with AutoCAD. The mixing multi-function chip and the frequency multiplier multi-function chip without a package cover is shown in Fig. 9. A large number of grounding vias are set around the cavity of the MMIC chip and the signal transmission line to ensure grounding continuity. Meanwhile, this design minimizes the mutual interference of microwave signals inside and outside the cavity and improves the electrom-

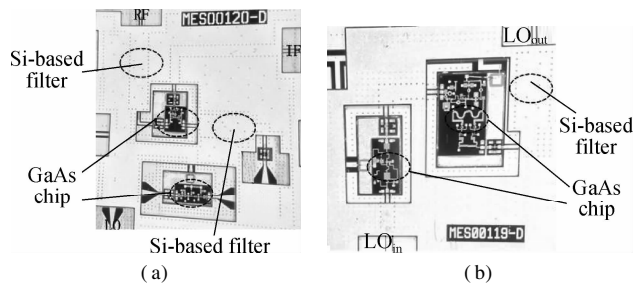


Fig. 9 The physical picture of the multi-function chips. (a) The mixing multi-function chip; (b) The frequency multiplier multi-function chip

agnetic compatibility of the multi-function chip.

The test results of the mixing multi-function chip and the frequency multiplier multi-function chip are shown in Tab. 1 and Tab. 2.

Tab. 1 Test results of the mixing multi-function chip

Specification	Min. value	Typical value	Max. value
Radio frequency f_{RF}/GHz	40		44
Local oscillator frequency f_{LO}/GHz	48		60
Intermediate frequency f_{IF}/GHz	6		18
Conversion gain G_c/dB	-18	-16	-15
Gain flatness $\Delta G_c/\text{dB}$		± 1	
LO-RF isolation I_{LO-RF}/dB	30	40	55
LO-IF isolation I_{LO-IF}/dB	20	30	50
Supply current I_{DD}/mA		80	
Chip size/(mm × mm × mm)		10 × 11 × 1	

Tab. 2 Test results of the frequency multiplier multi-function chip

Specification	Min. value	Typical value	Max. value
Input frequency f_{IN}/GHz	16		20
Output frequency f_{OUT}/GHz	48		60
Conversion gain G_{conv}/dB	12		14
Supply voltage V_{DD}/V		5	
Current I_D/mA		100	
Chip size/(mm × mm × mm)		8 × 8 × 1	

3.2 Test results of the broadband mixing component

As shown in Fig. 1, the mixing multi-function chip and the frequency multiplier multi-function chip are cascaded to form the broadband mixing component. The inter-stage also includes a pre-selector filter, an amplifier and an IF filter. The photo of the fully assembled mixing component is shown in Fig. 10.

A signal source is used to generate appropriate RF signals and LO signals to test the spur and gain from the output IF signal, as shown in Figs. 11-13. The overall spur is better than -50 dBc and the gain is better than 15 dB.

3.3 Comparison and analysis of test results

The comparison of the multi-function chip test results is shown in Tab. 3. It can be found that this paper presents

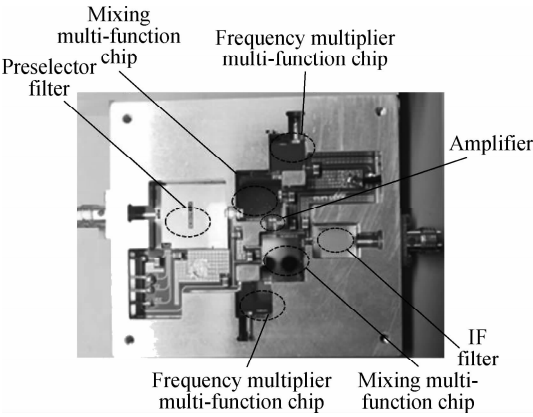


Fig. 10 Photo of the cascade broadband mixing component

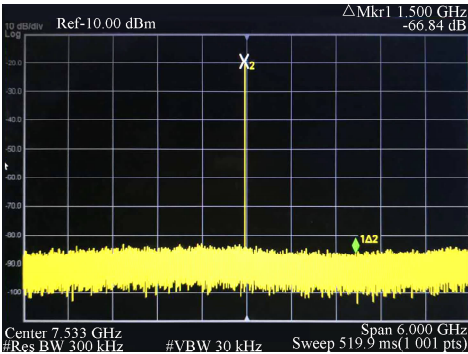


Fig. 11 Spur spectrum test results

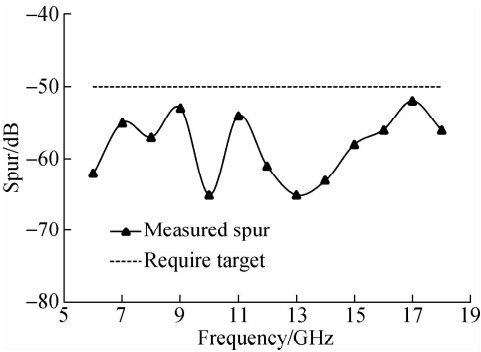


Fig. 12 Measured spur

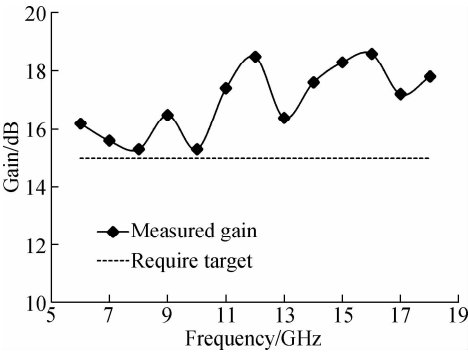


Fig. 13 Measured gain

3D heterogeneous integrated wideband RF chips based on silicon-based adapter board technology with complex integration, a compact size and wider bandwidth.

Tab.3 Comparison of the multi-function chips test results

Item	Transceiver module ^[2]	Transceiver SiP module ^[11]	This paper	
			Mixing multi-function chip	Frequency multiplier multi-function chip
Integration	Transceiver and antennas	RF front-end, ADC and DAC	Band-pass filter, mixer, attenuator, and amplifier	Frequency-tripler, band-pass filter and amplifier
Frequency/GHz	60	S and P band	40 to 44	48 to 60
Bandwith/GHz	1.76		4	12
Size/(mm × mm × mm)	6.5 × 6.5 × 0.6	38 × 40 × 4	10 × 11 × 1	8 × 8 × 1
Technology	TSV, ball grid array	Ball grid array	TSV, gold-gold bonding	TSV, gold-gold bonding

4 Conclusion

1) This paper adopted the silicon-based adapter board technology and implemented two multi-function chips. The mixing multi-function chip has a chip size of 10 mm × 11 mm × 1 mm. The RF frequency is 40-44 GHz, the IF covers the Ku band with greater than a 4 GHz instantaneous IF bandwidth. The frequency multiplier multi-function chip works in the 16-20 GHz frequency band, of which fundamental suppression is better than 50 dB and the second harmonic suppression is better than 40 dB, with a chip size of 8 mm × 8 mm × 1 mm.

2) The designed mixing multi-function chip and frequency multiplier multi-function chip are cascaded to form a broadband mixing component, which shows good test performance and can meet application requirements.

3) The proposed architecture combines 3D integration technologies such as SIP, SOP and POP to finally achieve a great improvement of the SWP to facilitate a broadband RF front-end system with excellent overall performances.

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基于硅转接板工艺的宽带射频芯片三维异构集成

王 勇^{1,2} 韦 炜² 杨 栋³ 孙 彪² 张兴稳² 张有明^{4,5} 黄风义^{4,5}

(¹东南大学信息科学与工程学院,南京 210096)

(²扬州船用电子仪器研究所,扬州 225001)

(³河北半导体研究所,石家庄 050002)

(⁴东南大学网络空间安全学院,南京 210096)

(⁵紫金山实验室,南京 211111)

摘要:基于硅转接板工艺实现了超宽带混频微系统组件的三维异构集成,该混频组件由混频多功能芯片和倍频多功能芯片级联而成. 基于晶圆级金-金键合工艺实现了四层高阻硅基板堆叠封装. 每一层均采用硅通孔 (TSV) 技术,从而实现信号之间的互连. 单片集成微波芯片 (MMIC) 嵌入在硅腔内,硅基滤波器集成在高阻硅衬底上. 硅基转接板上的互连线、腔体以及滤波器采用 AutoCAD 进行设计,并采用 HFSS 进行三维电磁场仿真. 根据测试结果,混频多功能芯片的射频频率为 40 ~ 44 GHz,中频频率可覆盖 Ku 频段,尺寸为 10 mm × 11 mm × 1 mm. 倍频多功能芯片工作在 16 ~ 20 GHz 频段,对基波信号的抑制优于 50 dB,对二次谐波信号的抑制优于 40 dB,尺寸为 8 mm × 8 mm × 1 mm. 级联后完全组装的混频组件可实现优于 -50 dBc 的杂散抑制比和优于 15 dB 的增益.

关键词:硅基转接板;混频;倍频;多功能芯片

中图分类号:TN389