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Non-inverting buck-boost DC-DC converter based on constant inductor current control

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Abstract: The hysteresis control combined with PWM control non-inverting buck-boost was proposed to improve the light load efficiency and power density. The constant inductor current control (CICC) was established to mitigate the dependence on the external components and device variation and make smooth transition between hysteresis control loop and pulse width modulation (PWM) control loop. The small signal model was deduced for the buck and boost operation mode. The inductor current slope control (ICSC) was proposed to implement the automatic mode transition between buck and boost mode in one switching cycle. The results show that the converter prototype has good dynamic response capability, achieving 94% efficiency and 95% peak efficiency at full 10 A load current.

Key words: four switch buck-boost converter; inductor current slope control; constant inductor current control; small signal model

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Battery is the most extensive use power supply in most applications, including electronic devices (mobile phone, wearable devices, etc.), automotive infotainment and start-stop system[1-2]. Battery voltage can be either greater or lower than the system operation voltage no matter it is charged or discharged. Thus, the implementation of non-inverting buck-boost converters is critical for regulating purpose. Compared with Sepic, Zeta and Flyback, four-switch buck-boost has much lower switch stress and magnetic element power loss, resulting in better EMI performance and higher power density. The traditional non-inverting buck-boost employs four switches with three-mode control to realize the up-down transition. However, since the hysteresis ΔV is introduced to avoid the fluctuation of the duty cycles, the line regulation performs not good enough when input voltage is close to output voltage[3]. Even with the compensation technique[4] or extra circuit like PLL[5], the dead zone still exists and the output voltage drops as the input voltage changes. The hybrid feed-forward control scheme[6-7] improves the line transient performance but needs input voltage sensing, one more dynamic sawtooth generator[8] and PWM comparator, which together make the system control more complicated[9]. Although hysteresis control could improve the efficiency in light load and load step response, the transition between hysteresis mode and PWM mode is not smooth or accurate due to the variation of external component parameters. The tradition hysteresis mode relies on the two non-overlap thresholds I_{LH} (load current from PWM to hysteresis) and I_{LP} (load current from hysteresis to PWM)[10]. The buck converter usually senses the inductor current as the load current and makes the decision by comparing with a reference current threshold. However, the inductor current of boost and buck-boost is related to the V_{in} and V_o. This paper proposes a constant inductor current control (CICC) method to make the operation mode transition smooth between hysteresis control mode and PWM control mode. Compared with the fixed transition current threshold, the CICC scheme decouples from the input and output voltage change and the parameter variation of external components.

In this paper, an inductor current slope control (ICSC) method is proposed to transit the operation mode between buck and boost in one switching cycle automatically so that it can mitigate both overshoot and undershoot of the output voltage when the input voltage changes.

1 System Architecture

The proposed buck-boost loop control architecture is composed of the hysteresis control loop and PWM control loop shown as Fig. 1. The hysteresis control loop is effective during light load while the converter transits to PWM control loop when the load increases. In hysteresis loop control, the CICC control block makes inductor current (I_L) operate between the peak current limit (I_p) and the zero current (I_{ZC}) until the output voltage (V_o) exceeds the rising threshold of the feedback hysteresis comparator (FHC). Then the converter works from the alive state to the sleep state, dramatically saving the controller loss and switching loss, and obviously improving the efficiency in light load condition. With the average inductor current ramping up, the valley inductor current increases gradually more than the zero current (I_{ZC}), leading to the converter transition from hysteresis mode to PWM mode. The CICC is proposed to make the peak to valley inductor

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current operate with a constant value as I_p, so that the control scheme can easily implement the smooth transition between hysteresis control loop and PWM control loop. The efficiency dip is eliminated at the mode transition point, compared with the traditional fixed inductor current transition threshold.

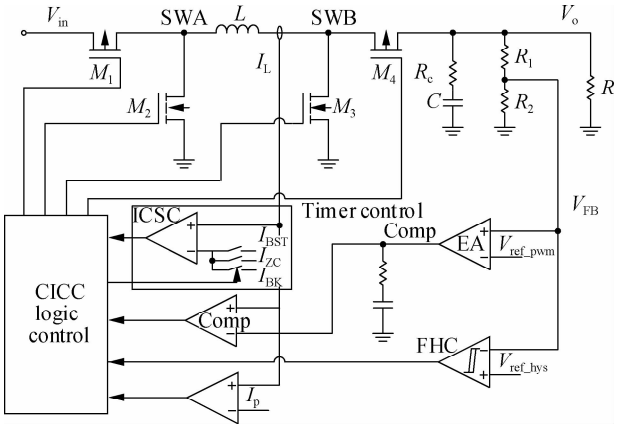

Fig. 1 The novel buck-boost control diagram

Both in hysteresis and PWM control, ICSC block senses I_L. With a given inductor, the slope of I_L is in proportion to the voltage across the inductor. $(V_{in} - V_o)/L$ is the common coefficient in buck-boost mode so that it can be a uniform input as the current slope comparator which determines the boost or buck mode in one switching cycle. ICSC can greatly improve the line regulation performance and improve the efficiency when the V_{in} is close to V_o.

2 System Implementation

2.1 Inductor current slope control (ICSC)

The state machine transition diagram of Fig. 2 shows the operation principle of ICSC. At the initial state, assuming that V_o is greater than the reference of the feedback hysteresis comparator (FHC), the converter is operating in the sleep state S1 with all switches off which are shown in Tab. 1. When the output signal of FHC turns to low, the converter transits to buck mode S3, in which M1 and M4 are turned on, if V_{in} is greater than V_o. When I_L exceeds I_p(PK = 1), the converter transits to mode S4, in which M2 and M4 are turned on. Until I_L is equal to the zero current (ZC = 1), the converter transits back to mode S3. As long as the FHC and C_{BST} keep low, I_L ramps up and down between zero current (I_{ZC}) and I_p. The C_{BST} is the output signal of the boost mode comparator with two inputs as of inductor current and boost mode current threshold I_{BST}, as shown in Fig. 3. When V_{FB} is higher than reference voltage V_{REF_HYS}, FHC goes high and the converter transits back to the sleep state S1.

When V_{in} becomes lower than V_o in S1 or S4 under buck mode, the converter changes to boost mode immediately in state S3 if only I_L is lower than the boost mode

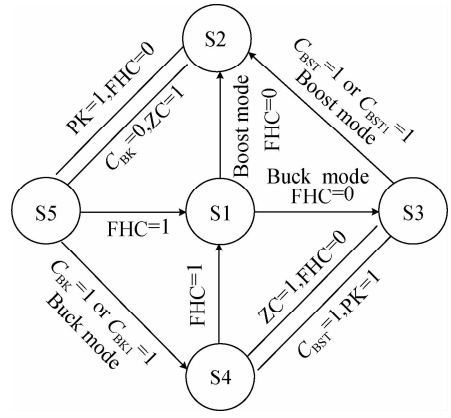

Fig. 2 ICSC operation state machine

Tab. 1 ICSC control scheme

State	M1	M2	M3	M4	Mode
S1	OFF	OFF	OFF	OFF	Sleep
S2	ON	OFF	ON	OFF	Boost
S3	ON	OFF	OFF	ON	Buck
S4	OFF	ON	OFF	ON	Buck
S5	ON	OFF	OFF	ON	Boost

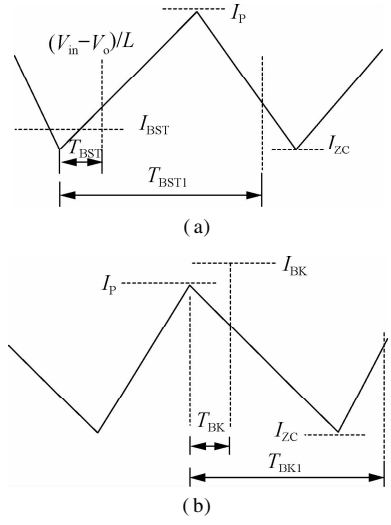

Fig. 3 Mode transition of inductor slope control. (a) Buck mode; (b) Boost mode

current threshold I_{BST} at the delay T_{BST}, since the rising slope of I_L is proportional to $V_{in} - V_o$ and can be inferred as the V_{in} and V_o relative level. When the V_{in} turns lower than V_o after the delay T_{BST} but before I_L hits I_p, the extra check at delay T_{BST1} is to assure that the converter changes to boost mode. At delay T_{BST1}, if I_L is still lower than I_p, the comparator output C_{BST1} transits to high and M1 is turned off. The converter changes to boost mode in the next switching cycle.

Under boost mode, the converter operates between S2 and S5 as I_L ramps up and down between the peak current I_p and zero current (I_{ZC}), if only FHC and C_{BK} keep low. C_{BK} is the output of the buck mode comparator, with two inputs as of the inductor current I_L and the buck mode current threshold I_{BK}. If V_{in} becomes higher than V_o in S1 or

S2, it transits to the buck mode immediately in state S5 when I_L is higher than I_{BK} at the delay T_{BK} since the falling slope of I_L is proportional to $V_o - V_{in}$ and can be inferred as the V_{in} and V_o relative level. If V_{in} becomes higher than V_o after the delay T_{BK} but before I_L hits I_{ZC}, the extra check at delay T_{BKI} is to assure that the converter changes to buck mode as well. At delay T_{BKI}, if I_L is still higher than I_{ZC}, the comparator output C_{BKI} transits to high and M4 is turned off. When V_{FB} is higher than the reference voltage V_{REF_HYS}, FHC goes high and the converter transits back to the sleep state S1.

Based on the control scheme analysis, these transitions of the operation mode are all completed in one switching cycle with ICSC control. Furthermore, V_o is charged up quickly and the converter goes to sleep state automatically as the IL slope is flat and the I_p is much larger than the load current. Therefore, compared with the conventional buck-boost without operation mode detection, there is no efficiency degraded when V_{in} is close to V_o.

The mode transition threshold of V_{in} and V_o level can be expressed as

$$(V_{in} - V_o)_{buck\rightarrow boost} = \frac{I_{BST}L}{T_{BST}} \tag{1}$$

$$(V_o - V_{in})_{boost\rightarrow buck} = \frac{I_{BK}L}{T_{BK}} \tag{2}$$

As voltage drops in M1 ~ M4, it is necessary to set the mode transition threshold for V_{in} slightly higher than V_o. The boost-to-buck threshold is larger than the buck-to-boost threshold to avoid glitches during mode transitions.

2.2 Constant peak and valley inductor current control

CICC is proposed as the constant peak and valley inductor current control scheme. It is not an external component dependent control scheme that can smoothly and accurately transit between hysteresis loop and PWM loop. In order to improve the efficiency and transient performance, the hysteresis control loop is more effective with light load. The inductor current ramps up and down between I_p and zero current until V_o exceeds the hysteresis window and then the converter goes into sleep mode to reduce the switching loss and controller loss. With the increase in the load current, V_o and V_{FB} drops gradually as the inductor current from peak to valley is constant. Meanwhile, the compensation node voltage of error amplifier increases to enlarge the load capability and PWM control loop is effective on the output regulation after 32 clock cycles. Finally, the reference voltage of hysteresis control and PWM control are adjusted simultaneously to cancel the load regulation under different control modes. Fig. 4 shows the control loop transition from hysteresis to PWM.

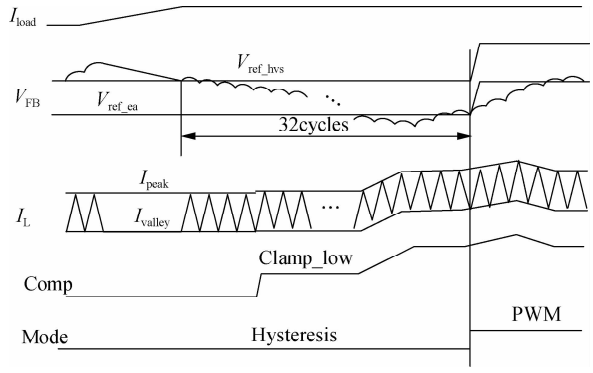

Fig. 4 Hysteresis to PWM mode transition of CICC

Similarly, the inductor current and compensation node voltage decrease as the load current decreases. The converter starts to skip switching pulses when V_{FB} goes higher than V_{REF_HYS} as the inductor current from peak to valley is constant. Meanwhile, the compensation node voltage of the error amplifier decreases and the hysteresis control loop is effective on the output regulation after 8 burst cycles. Finally, the reference voltage of hysteresis control and PWM control are adjusted simultaneously to cancel the load regulation under different control modes. Fig. 5 shows the control loop transition from PWM to hysteresis mode.

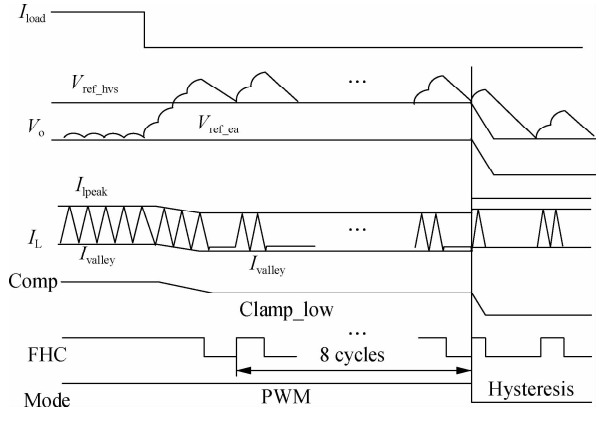

Fig. 5 PWM to hysteresis mode transition of CICC

Under the hysteresis mode, the hysteresis frequency is defined by the hysteresis window V_h, peak current I_p, input voltage V_{in}, output voltage V_o and load R.

$$f_{HYS} = \begin{cases} \dfrac{2(I_p/2 - V_o/R)V_o/R}{V_h C I_p} & \text{Buck} \\ \dfrac{2((1 - V_o/V_{in})I_p/2 - V_o/R)V_o/R}{V_h C I_p} & \text{Boost} \\ \dfrac{2[V_{in}I_p/(2V_o) - V_o/R]V_o/R}{V_h C I_p} & \text{Buck-boost} \end{cases} \tag{3}$$

Under PWM mode, the switching frequency varies with peak current I_p, input voltage V_{in}, output voltage V_o and inductance L.

$$f_{\mathrm{PWM}}=\begin{cases}\dfrac{V_{\mathrm{o}}(V_{\mathrm{in}}-V_{\mathrm{o}})}{V_{\mathrm{in}}I_{\mathrm{p}}L} & \text{Buck}\\ \dfrac{V_{\mathrm{in}}(V_{\mathrm{o}}-V_{\mathrm{in}})}{V_{\mathrm{o}}I_{\mathrm{p}}L} & \text{Boost}\\ \dfrac{V_{\mathrm{in}}V_{\mathrm{o}}}{(V_{\mathrm{in}}+V_{\mathrm{o}})I_{\mathrm{p}}L} & \text{Buck-boost}\end{cases} \tag{4}$$

2.3 Small signal model

As the switching frequency in PWM mode varies with load current, introduce t_{on} and t_{s} to replace duty d as the small signal variants,

$$t_{\mathrm{s}}=t_{\mathrm{on}}+t_{\mathrm{off}}=t_{\mathrm{on}}+L\frac{\Delta i_{\mathrm{L}}}{V_{\mathrm{o}}}=t_{\mathrm{on}}+L\frac{I_{\mathrm{p}}}{V_{\mathrm{o}}} \tag{5}$$

Solve it with small signal perturbation,

$$\hat{t}_{\mathrm{s}}=\hat{t}_{\mathrm{on}}+L\frac{I_{\mathrm{p}}}{V_{\mathrm{o}}}\approx\hat{t}_{\mathrm{on}}-L\frac{I_{\mathrm{p}}}{V_{\mathrm{o}}^2}\hat{v}_{\mathrm{o}}=\hat{t}_{\mathrm{on}}-\frac{(1-D)T_{\mathrm{s}}}{V_{\mathrm{o}}}\hat{v}_{\mathrm{o}} \tag{6}$$

Take buck mode as an example to deduce the small signal model,

$$t_{\mathrm{on}}=dt_{\mathrm{s}} \tag{7}$$

$$\hat{t}_{\mathrm{on}}=\hat{d}T_{\mathrm{s}}+D\hat{t}_{\mathrm{s}} \tag{8}$$

$$\hat{d}=\frac{(1-D)\hat{t}_{\mathrm{on}}+D(1-D)T_{\mathrm{s}}\hat{v}_{\mathrm{o}}/V_{\mathrm{o}}}{T_{\mathrm{s}}} \tag{9}$$

$$i_{\mathrm{p}}=\langle i_{\mathrm{L}}\rangle+\frac{\Delta i_{\mathrm{L}}}{2}=\langle i_{\mathrm{L}}\rangle+\frac{V_{\mathrm{in}}-V_{\mathrm{o}}}{2L}t_{\mathrm{on}} \tag{10}$$

$$\hat{i}_{\mathrm{p}}=\langle\hat{i}_{\mathrm{L}}\rangle+\frac{\hat{v}_{\mathrm{in}}-\hat{v}_{\mathrm{o}}}{2L}T_{\mathrm{on}}+\frac{V_{\mathrm{in}}-V_{\mathrm{o}}}{2L}\hat{t}_{\mathrm{on}} \tag{11}$$

$$\hat{t}_{\mathrm{on}}=\frac{2L}{V_{\mathrm{in}}-V_{\mathrm{o}}}\left(\hat{i}_{\mathrm{p}}-\langle\hat{i}_{\mathrm{L}}\rangle-\frac{DT_{\mathrm{s}}}{2L}\hat{v}_{\mathrm{in}}+\frac{DT_{\mathrm{s}}}{2L}\hat{v}_{\mathrm{o}}\right) \tag{12}$$

Substitute Eq. (12) to Eq. (9) and consider the current sense gain as R_{i}. $\hat{v}_{\mathrm{c}}$ is the output signal of the external voltage loop.

$$\hat{d}=\frac{2L}{V_{\mathrm{in}}T_{\mathrm{s}}R_{\mathrm{i}}}\left(\hat{v}_{\mathrm{c}}-R_{\mathrm{i}}\langle\hat{i}_{\mathrm{L}}\rangle-\frac{DT_{\mathrm{s}}R_{\mathrm{i}}}{2L}\hat{v}_{\mathrm{in}}+\frac{T_{\mathrm{s}}R_{\mathrm{i}}}{2LD}\hat{v}_{\mathrm{o}}\right) \tag{13}$$

According to the average model of the three-terminal device, the buck mode parameters of the CICC buck-boost can be defined as

$$F_{\mathrm{m}}=\frac{\hat{d}}{\hat{v}_{\mathrm{c}}}=\frac{2L}{V_{\mathrm{in}}T_{\mathrm{s}}R_{\mathrm{i}}}=\frac{2DD'}{I_{\mathrm{p}}R_{\mathrm{i}}} \tag{14}$$

$$F_{\mathrm{g}}=\frac{\hat{d}}{\hat{V}_{\mathrm{in}}}=-\frac{I_{\mathrm{p}}R_{\mathrm{i}}}{2V_{\mathrm{in}}D'} \tag{15}$$

$$F_{\mathrm{v}}=\frac{\hat{d}}{\hat{v}_{\mathrm{o}}}=\frac{I_{\mathrm{p}}R_{\mathrm{i}}}{2V_{\mathrm{o}}D'} \tag{16}$$

The CICC buck mode small signal switch model is shown as Fig. 6. Here $K_{\mathrm{i}}=1$ indicates it is the average inductor current control because peak current mode has the sample and hold delay in high frequency range that is $k_{\mathrm{i}}=H_{\mathrm{e}}(s)=1-s/(1/T_{\mathrm{s}})+s^2/(\pi/T_{\mathrm{s}})^2$. Therefore, the CICC mode is similar to the average current mode, but with better inner current loop response than peak current mode. The control-to-output transfer function is

$$\frac{\hat{v}_{\mathrm{o}}}{\hat{v}_{\mathrm{c}}}=\frac{R(sR_{\mathrm{c}}C+1)}{R_{\mathrm{i}}(T_{\mathrm{s}}s/2+1)(sRC+1)} \tag{17}$$

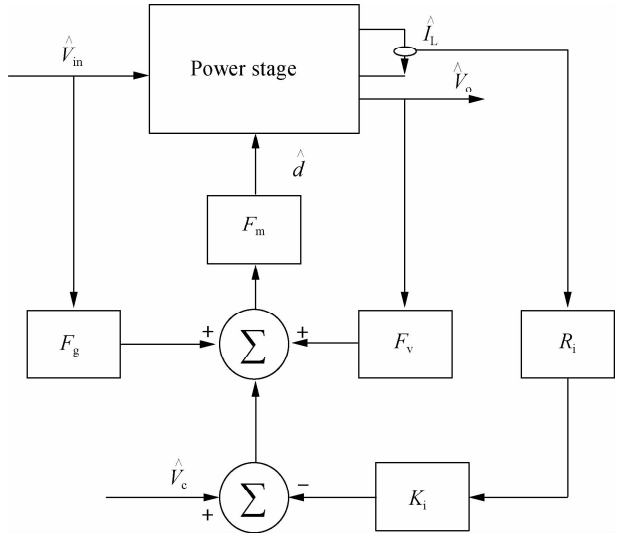

Fig. 6 Small signal model diagram of CICC buck mode

The loop modeling parameters of three operation modes are summarized in Tab. 2. It is easy to extend to control-to-output transfer function of the boost and buck-boost mode. Fig. 7 shows the control-to-output transfer function of buck and boost modes. These are both single pole systems so the converter keeps stable during the buck and boost mode transition.

Tab. 2 Loop modeling parameter summary

Operation mode	F_{m}	F_{g}	F_{v}
Buck	$\frac{2DD'}{I_{\mathrm{p}}R_{\mathrm{i}}}$	$-\frac{I_{\mathrm{p}}R_{\mathrm{i}}}{2V_{\mathrm{in}}D'}$	$\frac{I_{\mathrm{p}}R_{\mathrm{i}}}{2V_{\mathrm{o}}D'}$
Boost	$\frac{2DD'}{I_{\mathrm{p}}R_{\mathrm{i}}}$	$-\frac{I_{\mathrm{p}}R_{\mathrm{i}}}{2V_{\mathrm{o}}DD'}$	$\frac{I_{\mathrm{p}}R_{\mathrm{i}}}{2V_{\mathrm{o}}D}$
Buck-boost	$\frac{2DD'}{I_{\mathrm{p}}R_{\mathrm{i}}}$	$-\frac{I_{\mathrm{p}}R_{\mathrm{i}}D}{2V_{\mathrm{o}}D'}$	$\frac{I_{\mathrm{p}}R_{\mathrm{i}}}{2V_{\mathrm{o}}}$

3 Experimental Results

Wide output voltage range (6-36 V) and input voltage (5-40 V) are achieved with 10 A maximum load current (2.4 A). The prototype specifications are listed in Tab. 3. The typical output voltage is 12 V with 2.4 A peak to valley I_{L}. With ICSC control, the converter is operating in buck mode with 36 V V_{in}, in boost mode with 6 V V_{in} and in buck-boost mode with $12V_{\mathrm{in}}$. When the voltage difference is small between V_{in} and V_{o}, switch M1 and

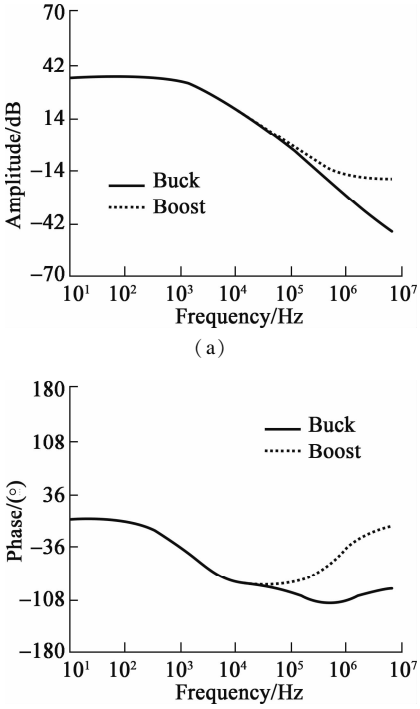

Fig. 7 Control-to-output transfer function of CICC buck-boost converter. (a) Amplitude; (b) Phase

Tab. 3 Prototype specifications

Parameter	Value
V_{in}/V	5-40
V_o/V	6-36
Inductor/μH	2.2
Output capacitor/μF	100
Error amplifier gain/μS	660
Current sense resistor/mΩ	2
Compensation resistor/kΩ	30
Compensation capacitor/nF	2.2

switch M4 are almost always on during the switching phase until V_o is charged to larger than the reference rising threshold of the hysteresis comparator.

The load transient response is shown in Fig. 8. The load step is 5 A, the half of the full load with 1 A/μs slew rate. The output voltage deviations are all less than 4%. Fig. 9 is the line transient response. The maximum output voltage deviation is 3.8% with 7 to 18 V line transient and 0.1 V/μs slew rate.

Fig. 10 illustrates the conversion efficiency in different V_{in}. The peak efficiency reaches 95% and the full load efficiency is 94%. Furthermore, the efficiency is greater than 76% when the load current is more than above 10 mA.

4 Conclusion

1) A novel ICSC non-inverting buck-boost converter with automatic and fast buck and boost mode transition in one switching cycle is proposed in this paper. The converter avoids the output voltage fluctuation with small output ripple.

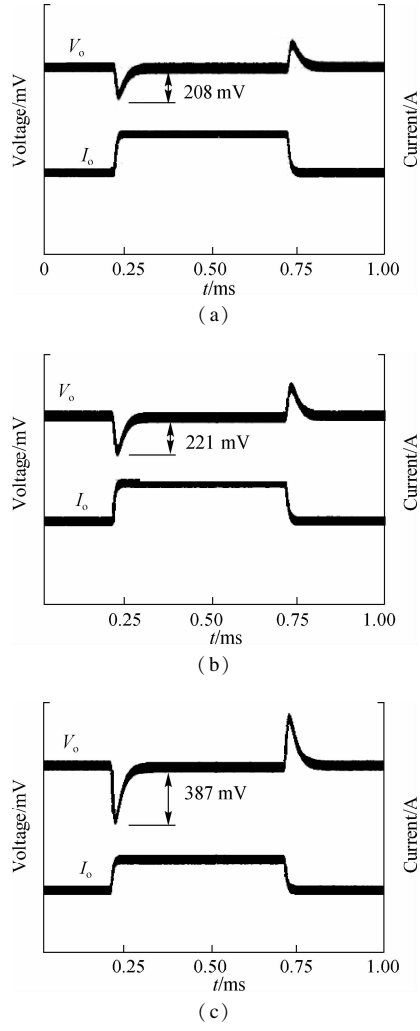

Fig. 8 Measured load transient performance. (a) V_{in} = 36 V; (b) V_{in} = 12 V; (c) V_{in} = 6 V

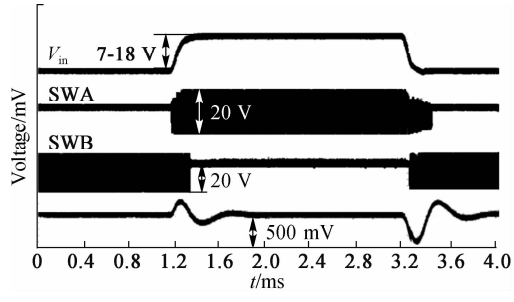

Fig. 9 Measured line transient performance

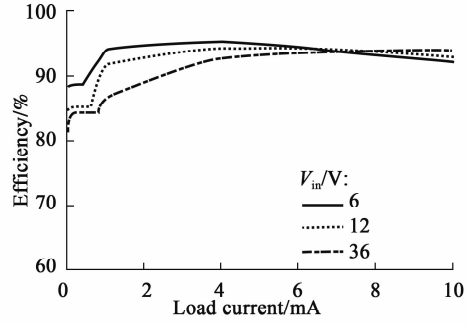

Fig. 10 Measured efficiency

2) With the CICC control, the converter can also smoothly transit between hysteresis loop and PWM loop. The stability is verified with small signal analysis.

3) The load transient response measurement shows less than 4% deviation with half of full load step. It achieves the 95% peak efficiency and 94% efficiency at full 10 A load.

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基于恒电感电流控制的非反相升降压 DC-DC 变换器

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摘要:为提高升降压变换器的轻载效率和功率密度,提出了一种迟滞控制结合 PWM 控制的非反相升降压变换器.设计出基于恒定电感电流的控制模式以减少对外部元器件的依赖性,并实现迟滞控制回路和 PWM 控制回路之间的平滑切换.针对降压和升压的工作模式推导出小信号模型,采用电感电流斜率的控制方法实现在一个开关周期内降压和升压模式之间的自动模式转换.结果表明,该变换器原型具有良好的动态响应能力,在满负载 10 A 电流下实现了 94% 的效率和 95% 的峰值效率.

关键词:四开关升降压转换器;电感电流斜率控制;恒电感电流控制;小信号模型

中图分类号:TM46