

Design of millimeter-wave reflective attenuators with capacitive compensation technique

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Abstract: To improve the attenuation accuracy and phase variation performance, two 5-bit millimeter-wave reflective attenuators with a capacitive compensation technique in gallium arsenide (GaAs) pseudomorphic high-electron-mobility transistor (PHEMT) process are presented. The parasitic effect of a millimeter-wave switch can be absorbed effectively in the design of the reflection load with capacitive compensation. Thus, attenuation and phase accuracy can be improved. Three basic capacitive compensation topologies were presented, and based on the analysis of the reflection coefficient on the Smith chart, the corresponding attenuation and phase variation were given. Furthermore, the design flow and optimization method of the reflective attenuator based on the capacitive compensation technique were summarized. Both chips are integrated with a 5-bit attenuator and a single-pole double-throw (SPDT) switch, and the chip size is 3 mm × 1 mm. Chip A with tail capacitance compensation was fabricated by a 0.5 μm GaAs PHEMT process, and Chip B with the compensation of the shunt capacitors before and after the switch was fabricated by a 0.15 μm GaAs PHEMT process. For both chips, the insertion loss (IL) with the SPDT switch is less than 4.5 dB, the IL of the 5-bit attenuator is less than 3 dB, the root-mean-square attenuation error is less than 0.4 dB, and the input 1 dB gain compression power is greater than 25 dBm. The phase variations of Chips A and B are less than ±5° and ±2.5°, respectively.

Key words: reflective attenuators; millimeter-wave; capacitive compensation; low attenuation error; low phase variation

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The active phased-array technique has been widely used in radar and millimeter-wave communication applications^[1]. The attenuator is a key building block in a millimeter-wave phased-array system, which is used to compensate for gain error by controlling the gain and suppress the side-lobe level by adjusting the signal ampli-

tude^[2]. Meanwhile, the attenuator should have a low phase variation over different attenuated states to minimize the tracking error and reduce the difficulty of calibration^[1-3].

In the passive digital step attenuator (DSA), five topologies, namely, distributed, switched-path, switched T/π, bridged-T/π, and reflective attenuators, have been investigated in Refs. [1, 4-5]. Distributed attenuators have a wide bandwidth and low insertion loss (IL) but have a low attenuation range and large chip size^[6-8]. Switched-path attenuators have low amplitude and phase variations but often suffer from high IL and large chip sizes because of the use of many switches and transmission lines^[9-10]. Switched T/π and bridged-T/π attenuators have a low IL, high maximum attenuation, and compact size. However, they still have a relatively large attenuation and phase variation in wideband applications. Reflective attenuators exhibit competitive performance compared with other topologies with extremely low loss, wideband input/output matching, and sufficient attenuation range^[5, 11-12]. The use of a passive coupler increases the chip size, which is generally acceptable in millimeter-wave. The main challenge is the parasitic effect of switches on the reflection load, which makes it difficult to obtain accurate attenuation and low phase error concurrently^[11-13].

In this paper, we present effective design and optimization methods using a capacitive compensation technique to cope with the design challenge of a reflective attenuator. Two 5-bit millimeter-wave reflective attenuators in the gallium arsenide (GaAs) PHEMT process have been implemented, achieving low IL, excellent root-mean-square (RMS) attenuation error, and RMS phase error.

1 Design Flow and Optimization Method

1.1 Principle of a reflective attenuator

The topology of the reflective attenuator is shown in Fig. 1, which consists of a 4-port network and two 2-port networks. Ports 2 and 3 of the 4-port network are connected to the same adjustable load, and the reflection coefficient is Γ . With the load changes, the transmission coefficients between the input port (Port 1) and the output port (Port 4) are different, which can be designed to be

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the reference and attenuated states, respectively. In the monolithic microwave integrated circuit (MMIC) design, a Lange or hybrid coupler is widely used as a 4-port network, which is also called a 3 dB directional coupler^[11-12].

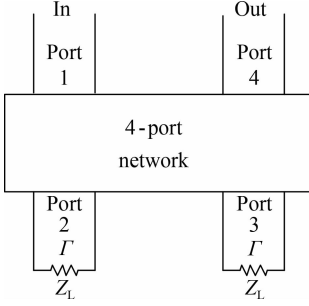


Fig. 1 Topology of the reflective attenuator

The S parameter of a matched and reciprocal coupler is expressed as follows^[5]:

$$S = \begin{bmatrix} 0 & \alpha & j\beta & 0 \\ \alpha & 0 & 0 & j\beta \\ j\beta & 0 & 0 & \alpha \\ 0 & j\beta & \alpha & 0 \end{bmatrix} \quad (1)$$

where α is the coupling coefficient from the input port (Port 1) to the coupling port (Port 3); β is the coupling coefficient from the input port (Port 1) to the through port (Port 2).

Based on the signal flow diagram, the S parameter of the reflective attenuator can be derived as follows:

$$S = \begin{bmatrix} (\alpha^2 - \beta^2)\Gamma & j2\alpha\beta\Gamma \\ j2\alpha\beta\Gamma & (\alpha^2 - \beta^2)\Gamma \end{bmatrix} \quad (2)$$

For a lossless coupler, $\alpha^2 + \beta^2 = 1$; in particular, for the 3 dB directional coupler, $\alpha = \beta = 1/\sqrt{2}$. Then, the S parameter of the reflective attenuator can be simplified as follows^[11]:

$$S = \begin{bmatrix} 0 & j\Gamma \\ j\Gamma & 0 \end{bmatrix} \quad (3)$$

If the 3 dB coupler is reciprocal and matched ideally, then the return loss of the attenuator in the reference and attenuated states will be 0. The IL I_L , attenuation A_u , and phase variation θ are derived as follows:

$$I_L = |S_{21,R}| = |\Gamma_R| = \left| \frac{Z_R - Z_0}{Z_R + Z_0} \right| \quad (4)$$

$$A_u = |S_{21,A}| - |S_{21,R}| = |\Gamma_A| - |\Gamma_R| \quad (5)$$

$$\theta = \angle S_{21,A} - \angle S_{21,R} = \angle \Gamma_A - \angle \Gamma_R \quad (6)$$

1.2 Calculation of the initial value of load impedance

Theoretically, with the reflection coefficient increasing from 1 to 0, the IL of the attenuator varied from 0 to infinity. For the desired attenuation value, the attenuation

and phase variation equation should be satisfied across the frequency band as follows:

$$\left. \begin{aligned} \theta(\omega) &= \angle \Gamma_A(\omega) - \angle \Gamma_R(\omega) = 0 \\ A_u(\omega) &= |\Gamma_A|(\omega) - |\Gamma_R|(\omega) = \text{constant} \end{aligned} \right\} \quad (7)$$

Let the load impedance be pure resistance, with the reflection coefficient Γ changing between 1 (reference state) and $10^{-x/20}$ (attenuated state). The IL of the attenuator is 0 dB and the attenuation is x dB. Ideally, the load resistance can be derived as follows^[5,11]:

$$R_L = Z_0 \frac{10^{-x/20} - 1}{10^{-x/20} + 1} \text{ or } Z_0 \frac{10^{-x/20} + 1}{10^{-x/20} - 1} \quad (8)$$

The relationship between attenuation and normalized R_L is shown in Fig. 2. When R_L becomes close to 50 Ω , the attenuation is approximately infinity. Two different values of load resistance, one is greater than 50 Ω and the other less than 50 Ω , can lead to the same attenuation. Compared with a load resistance of less than 50 Ω , a load resistance of greater than 50 Ω can make the attenuation change more smooth. The attenuation becomes extremely sensitive to the load resistance if the attenuation value is greater than 20 dB^[11]. In particular, when the load resistance value is 0 or infinity, the reflection coefficient will be 1, and the IL of the reference state will be 0 dB. Although the switch in the MMIC design exhibits on-state resistance and off-state capacitance, it is difficult to obtain 0 load resistance, and an off-state switch can make the load resistance close to infinity. To improve the accuracy and consistency of the attenuator, the attenuation of the reflective attenuator should be less than 20 dB, and the load impedance should be greater than 50 Ω .

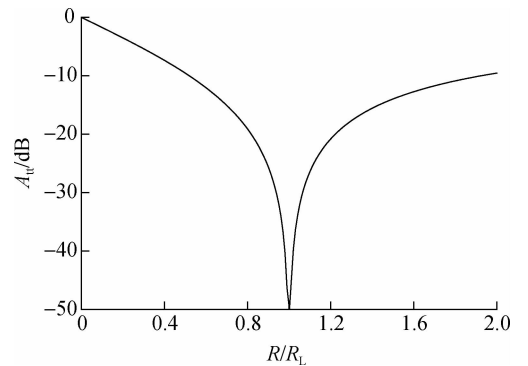


Fig. 2 Relationship between normalized R_L and attenuation

1.3 Design of load impedance

The scalable model of the PHEMT switch based on analysis of the physical structure can well fit the measured small-signal characteristics. To facilitate the theoretical derivation in the MMIC design, a simplified model with four main parameters, namely, on-state resistance R_{on} , off-state capacitance C_{off} , off-state resistance R_{off} , and

parasitic inductance L introduced by the transmission line in the transistor, is used. These four parameters are proportional to the total gate width of the switch transistor. The larger the total gate length, the smaller R_{on} is, which means that the IL of the switch is smaller.

However, a large C_{off} makes the isolation of the switch decrease with the increase in frequency. In particular, in the millimeter-wave design, the characteristics of the two states are similar, which means that a large gate length switch should not be chosen in the design of the micro-wave control circuit. When C_{off} is small, the contribution of reactance in series with C_{off} in the reflective load can be ignored. Therefore, the reflection coefficient of the attenuator in the reference state is mainly determined by C_{off} , and the reflection coefficient is located near the circle of the $\Gamma = 1$ Smith chart. Then, in the attenuated state, the reflection coefficient of the load needs to be located at the equal reflection coefficient circle near the origin to satisfy Eq. (7).

Using the Smith chart, the design goal is visualized. The reflected impedance of two states can form concentric arcs with the origin as the center over the operating frequency band. In the GaAs PHEMT process, the on-resistance of the switch with a minimum gate length is less than 50Ω . Therefore, the series resistance provides the most effective way to move the reflected impedance to the right half circle of the Smith chart while introducing only a few parasitic Effects.

1.4 Capacitive compensation technique

Design challenges to millimeter-wave reflective attenuators originate from the parasitic effect of switches. The series resistance makes the reflected impedance move closer to the target design range, and the phase of the reflection load should be compensated for to form concentric arcs. Both inductance and capacitance can be used for phase compensation. Given the order of magnitude of parasitic inductance and capacitance, the phase compensation devices should be carefully designed. The inductance of this level cannot guarantee implementation accuracy^[11], whereas the capacitance of this level, which is implemented as metal-oxide-metal, metal-insulator-metal, or open microstrip line, can be relatively accurate.

Three basic capacitive compensation topologies are presented in Fig. 3, which include the series tail capacitance C_s , the shunt capacitor C_B connected to the ground before the switch, and the shunt capacitor C_F connected to the ground after the switch. Variations of the reflected impedance with capacitance tuning of two states are discussed.

For the topology shown in Fig. 3(a), the reflected impedance of two states can be determined as follows:

$$\left. \begin{aligned} Z_A(\omega) &= \frac{1}{j\omega C_s} + R_L + R_{on} + j\omega L \\ Z_R(\omega) &= \frac{1}{j\omega C_s} + R_L + R_{off} + \frac{1}{j\omega C_{off}} + j\omega L \end{aligned} \right\} \quad (9)$$

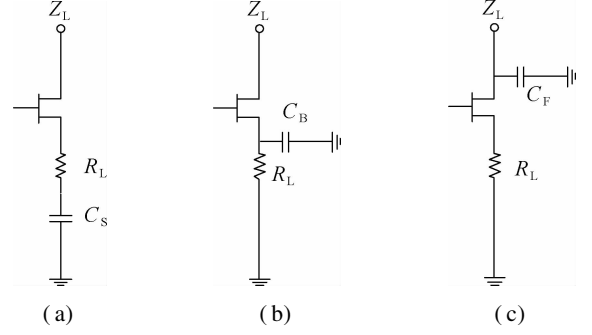


Fig. 3 Schematic of the proposed basic capacitive compensation topologies. (a) With tail capacitance C_s ; (b) With shunt capacitor C_B ; (c) With shunt capacitor C_F

where R_{on} is the on-state resistance; C_{off} is the off-state capacitance; R_{off} is the off-state resistance; and L is the parasitic inductance.

The tail capacitance C_s is two orders of magnitude larger than C_{off} . As shown in Fig. 4(a), the contribution of C_s to the reflected impedance in the reference state can be ignored. Therefore, C_s can hardly affect the IL and phase of the reference state. By contrast, in the attenuated state, as C_s increases, the reflected impedance moves into the capacitive semicircle and rotates counterclockwise along the equal impedance circle on the Smith chart, which means that a larger C_s leads to a phase lag in the attenuated state.

For the topology shown in Fig. 3(b), the reflected impedance of two states can be determined as follows:

$$\left. \begin{aligned} Z_A(\omega) &= R_L \left\| \frac{1}{j\omega C_B} + R_{on} + j\omega L \right. \\ Z_R(\omega) &= R_L \left\| \frac{1}{j\omega C_B} + R_{off} + \frac{1}{j\omega C_{off}} + j\omega L \right. \end{aligned} \right\} \quad (10)$$

Notably, the contribution of the shunt capacitor C_B connected to the ground after the switch to the reflected impedance in the reference state can also be ignored. As shown in Fig. 4(b), in the attenuated state, as C_B increases, the reflected impedance moves into the capacitive semicircle and rotates clockwise around the initial load impedance point on the Smith chart, which means that a larger C_B also leads to a phase lag in the attenuated state.

The shunt capacitor C_F connected to the ground before the switch has a considerable influence on the reflected impedance in both the reference and attenuated states. For the topology shown in Fig. 3(c), the reflected impedance of two states can be determined as follows:

$$\left. \begin{aligned} Z_A(\omega) &= (R_{on} + j\omega L + R_L) \left\| \frac{1}{j\omega C_F} \right. \\ Z_R(\omega) &= \left(R_{off} + \frac{1}{j\omega C_{off}} + j\omega L + R_L \right) \left\| \frac{1}{j\omega C_F} \right. \end{aligned} \right\} \quad (11)$$

As shown in Fig. 4(c), in the attenuated state, as C_F

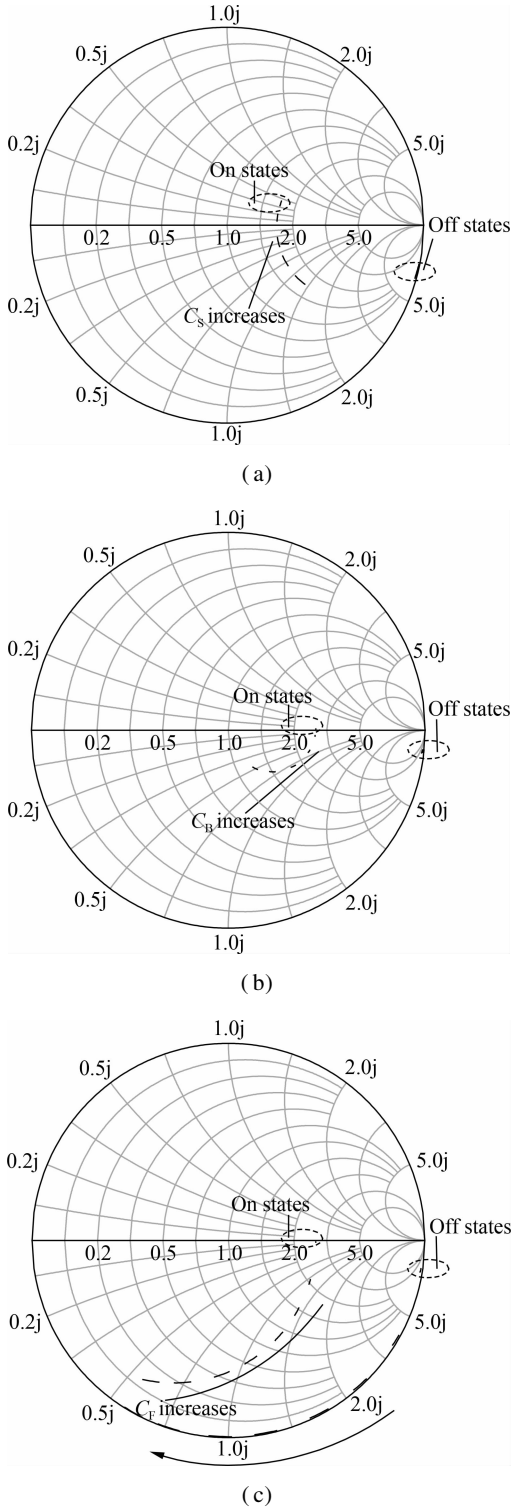


Fig. 4 Variation of reflected impedance on the Smith chart. (a) With tail capacitance C_s ; (b) With shunt capacitor C_B ; (c) With shunt capacitor C_F

increases, the reflected impedance moves into the capacitive semicircle and rotates clockwise along the equal admittance circle on the Smith chart. In the reference state, the reflected impedance also rotates clockwise along the equal admittance circle but with a different phase shift speed.

$$\left. \begin{aligned} Z_A(\omega) &= \left(R_L \left\| \frac{1}{j\omega C_B} + R_{on} + j\omega L \right\| \left\| \frac{1}{j\omega C_F} \right\| \right) \\ Z_R(\omega) &= \left(R_L \left\| \frac{1}{j\omega C_B} + \frac{1}{j\omega C_{off}} + R_{off} + j\omega L \right\| \left\| \frac{1}{j\omega C_F} \right\| \right) \end{aligned} \right\} \quad (12)$$

A reflective attenuator with compensation of the shunt capacitors C_B and C_F can be effectively designed. The reflected impedance of the two states is expressed in Eq. (12). Remarkably, as C_F increases, the phase difference between the two states changes from phase lag to phase lead. For example, in practical design, the size of the switch is $2 \times 20 \mu\text{m}/0.15 \mu\text{m}$ in a $0.15 \mu\text{m}$ GaAs PHEMT process. The relationship between phase error and C_F with different C_B is shown in Fig. 5. Let the design of C_F be in the phase lead range. Then, shunt capacitors C_B and C_F in one attenuation unit can adjust the phase error in opposite directions, which is useful in the fine-tuning of chip applications.

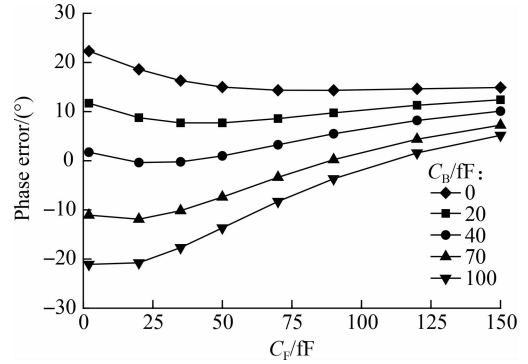


Fig. 5 Relationship between phase error and C_F with different C_B

2 Implementation and Measurement Results

To demonstrate the effectiveness of the proposed capacitive compensation technique, two 5-bit millimeter-wave reflective attenuators were utilized. In Fig. 6, Chip A with compensation of the tail capacitor C_s and Chip B with compensation of the shunt capacitors C_B and C_F are presented.

2.1 Chip A with compensation of the tail capacitor

If the parasitic effect of the switches decreases, then there is sufficient compensation of the reflective attenuator with only tail capacitance C_s . This means that the reflected impedance has a wide bandwidth and is suitable for small attenuation with small gate length switches, particularly when the process node is relatively backward. Compensation of the tail capacitor C_s applies to the design of attenuation smaller than 4 dB. An advantage of the topology is that C_s with larger capacitance is insensitive to process variations.

Based on the analysis, the design flow for a reflective

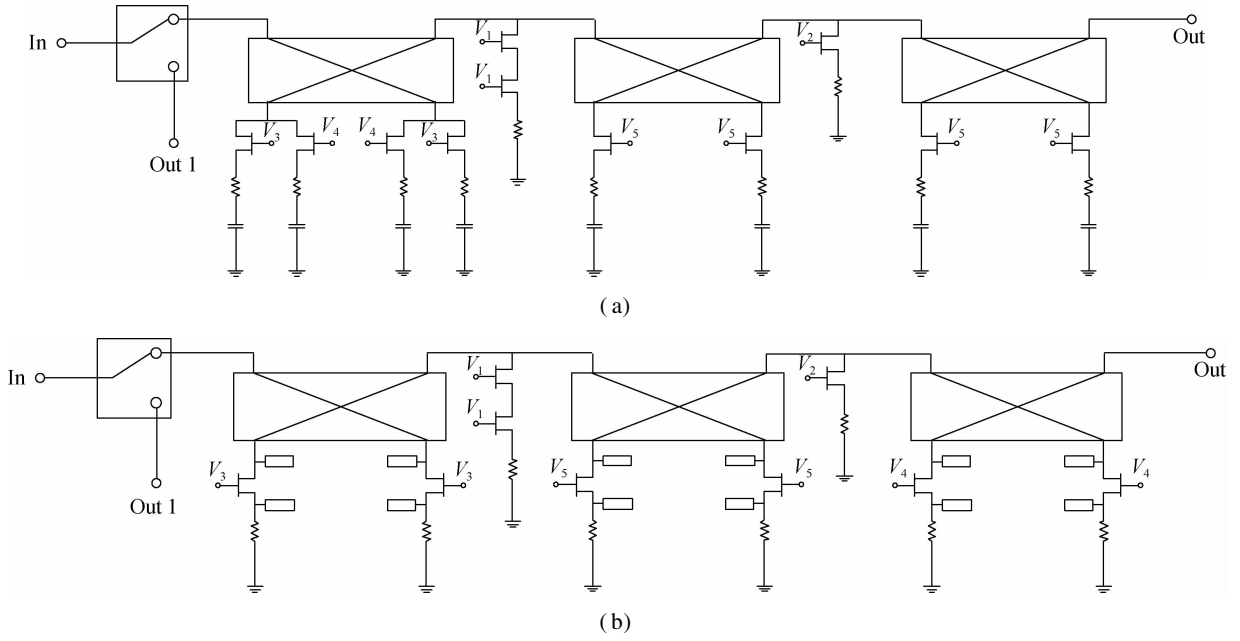


Fig. 6 Schematic of the proposed 5-bit reflective attenuators with a single-pole double-throw (SPDT) switch. (a) Chip A; (b) Chip B

attenuator with compensation of tail capacitor C_s can be summarized as follows: Firstly, given the design attenuation, the gate length of the switch and the equivalent parasitic parameters are determined. Secondly, according to Eqs. (7) and (9), the parameters of C_s and R_L at the central frequency point can be calculated. Thirdly, given the initial parameters, the electromagnetic (EM) co-simulation and optimization are performed with a circuit simulator and high-frequency structure simulator.

In this topology, although the attenuation and phase variation equation are satisfied only at the central frequency point, small attenuation and phase errors are maintained in a wider frequency band because of the small parasitic effect, which can meet the design requirements.

Chip A consists of a 5-bit attenuator and a single-pole double-throw (SPDT) switch in series. As shown in Fig. 6(a), the 8 dB attenuation unit in Chip A is composed of two 4 dB attenuation units in the cascade, the 4 and 2 dB attenuation share the same Lange coupler, and all tail capacitors are implemented in the form of interdigital capacitor. Chip A shows that a millimeter-wave broadband attenuator with good performance can be implemented in the GaAs PHEMT process of a backward node. However, the units with larger attenuation, such as 8 and 16 dB, cannot be implemented based on the topology, which instead can be cascaded by small attenuation units.

2.2 Chip B with compensation of the shunt capacitors C_B and C_F

For the topology of compensation with two capacitive variables, the attenuation and phase variation equation can be satisfied at a wide band of frequencies. As shown in Fig. 6(b), the 8, 4, and 2 dB attenuation units in Chip

B adopt the same topology of compensation of the shunt capacitors C_B and C_F . Given chip implementation and tuning, all shunt capacitors were implemented in the form of open microstrip lines.

Similarly, the design flow for a reflective attenuator with compensation of the shunt capacitors C_B and C_F can be summarized as follows: Firstly, given the design attenuation, the total series resistance is determined. Secondly, the initial parameters of the gate length of switches and load resistance R_L are chosen, which makes R_{on} nearly equal to R_L . Secondly, according to Eqs. (7) and (12), the parameters of C_B and C_F at the central frequency point can be calculated. Thirdly, given the initial parameters, the EM co-simulation and optimization are performed with a circuit simulator and high-frequency structure simulator.

2.3 Measurement results

Chip A with tail capacitor compensation is fabricated in a 0.5 μm GaAs PHEMT process. Chip B with compensating shunt capacitors C_B and C_F is fabricated in a 0.15 μm GaAs PHEMT process. The micrographs of Chips A and B are shown in Fig. 7, with the total chip size of both being 3 mm \times 1 mm. The chips were measured on a high-frequency probe station, and the simulated and measured performances were compared.

The performance of Chip A is shown in Figs. 8 to 10, with input and output voltage standing wave ratio (VSWR) less than 1.5, IL of the standalone switch of 1.5 dB, IL with a switch of 3.5 dB, RMS amplitude error less than 0.4 dB, RMS phase error less than 5°, and phase variation of $\pm 5^\circ$ in the working frequency band of 30 to 40 GHz.

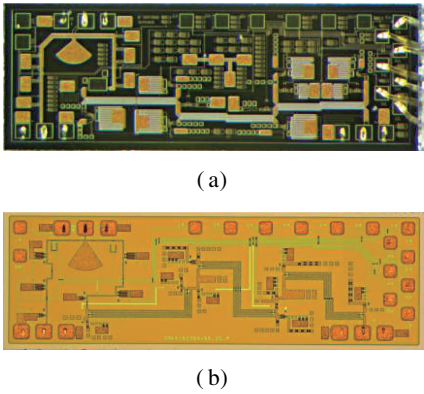


Fig. 7 Micrographs of the proposed chips. (a) Chip A; (b) Chip B

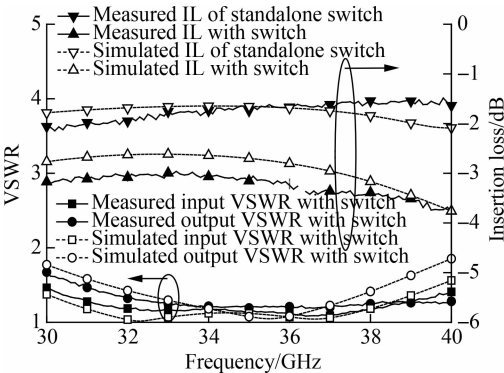


Fig. 8 VSWR and IL of Chip A

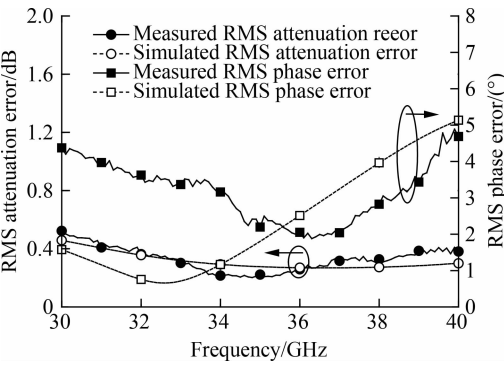


Fig. 9 RMS attenuation error and phase error of Chip A

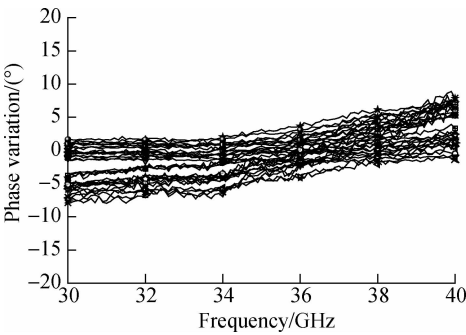


Fig. 10 Phase variation of Chip A

The performance of Chip B is shown in Figs. 11 to 13, with input and output VSWR less than 1.5, IL of the standalone switch of 1.5 dB, IL with a switch of 4 dB, RMS attenuation error less than 0.4 dB, RMS phase error less than 1.5°, and phase variation of $\pm 2.5^\circ$ in the working frequency band of 30 to 40 GHz. As shown in Fig. 14, the input 1 dB gain compression power($P_{1\text{ dB}}$) is greater than 25 dBm for both chips.

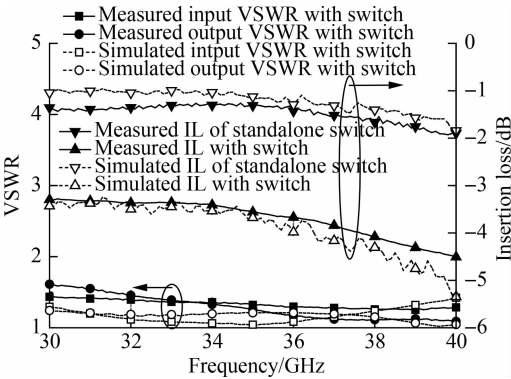


Fig. 11 VSWR and IL of Chip B

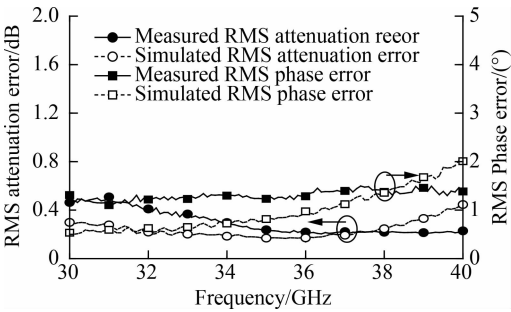


Fig. 12 RMS amplitude and phase errors of Chip B

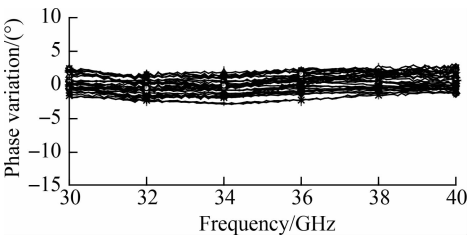


Fig. 13 Phase variation of Chip B

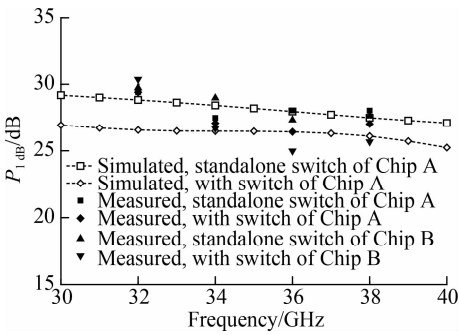


Fig. 14 Input 1 dB gain compression power of Chips A and B

Tab. 1 compares Chips A and B with the prior state-of-the-art DSAs. As shown in Tab. 1, reflective attenuators in both compound and silicon-based semiconductor processes show significant advantages of low loss^[11–12].

The reflective attenuators utilizing the presented capacitive compensation technique exhibit better attenuation and phase accuracy than other attenuators.

Tab. 1 Performance comparison with state-of-the-art digital step attenuators

Method	Frequency/ GHz	Technique	IL/dB	Return loss/dB	Attenuation range/dB	RMS attenuation error /dB	RMS phase error /(°)	P_1 dB/ dBm	Type	Size/ (mm × mm)
TMTT' 18 ^[9]	6-18	0.25 μm GaAs PHEMT	<9	>10	31.5(6 bit) (LSB = 0.5 dB)	<0.6	Phase variation < ± 7.0°	N/A	Switched T/ path	2.7 × 2.0
MMWCST' 13 ^[14]	19-23	0.1 μm GaAs PHEMT	3.9	>11	31.5(6 bit) (LSB = 1 dB)	N/A	P_1 dB variation < ± 5.0°	N/A	Bridged-T/π	3.0 × 2.0
EUCAP' 19 ^[10]	20-32	0.25 μm GaAs PHEMT	18 with Phase shifter	>12	23.625(6 bit) (LSB = 0.25 dB)	0.5	<2.8	N/A	Switched T/ path	1.0 × 0.8
MTTS' 16 ^[15]	25-30	0.15 μm GaAs PHEMT	5.7	>10	31.5(6 bit) (LSB = 0.5 dB)	<0.21	Phase variation < ± 6.0°	N/A	Bridged-T/π	2.0 × 1.0
MWCL' 21 ^[16]	28-40	0.13 μm SiGe BiCMOS	5.4-9.1	10	31(5 bit) (LSB = 1 dB)	0.43	5.4	15.7@ 35 GHz	Bridged-π with inductive compensation	0.21
VLSI' 21 ^[12]	33-41	0.13 μm SiGe BiCMOS	<13	>10	15.5(5 bit) (LSB = 0.5 dB)	0.2	<2.5	17.5	Bridged-T/π	0.22
TCS' 20 ^[4]	37-40	65 nm CMOS	7	>12	31(5 bit) (LSB = 1 dB)	<0.27	<3.7	12	Bridged-T/π with tail capacitor	0.21
SEU' 18 ^[11]	30-35	0.15 μm GaAs PHEMT	3.7	>9	31(5 bit) (LSB = 1 dB)	<0.85	8@ 30-33 GHz	24.6@ 31 GHz	Reflective attenuator with resonant inductor	0.9 × 2.0
APMC' 14 ^[17]	40-50	0.15 μm GaAs PHEMT	6.5@ 40 GHz	>10	31.5(6 bit) (LSB = 0.5 dB)	0.5	N/A	N/A	Bridged-T/π	1.8 × 1.1
Proposed	Chip A	0.5 μm GaAs PHEMT	3 *	>15	15.5(5 bit) (LSB = 0.5 dB)	0.4	<5	>25	Reflective attenuator with tail capacitor	1.8 **
	Chip B	0.15 μm GaAs PHEMT	3 *	>15	15.5(5 bit) (LSB = 0.5 dB)	0.4	<1.5	>25	Reflective attenuator with shunt capacitor	1.8 **

Notes: * Calculated IL of the standalone attenuator with measured results; ** chip size of the standalone attenuator.

3 Conclusions

1) Three basic capacitive compensation topologies were presented and analyzed. The design flow and optimization method of a reflective attenuator based on the capacitive compensation technique are summarized.

2) Two 5-bit millimeter-wave reflective attenuators with the capacitive compensation technique in the GaAs PHEMT process are presented. The measured results can well verify the circuit simulation for both chips.

3) Capacitive compensation with a tail capacitor is suitable for small attenuation units, and larger attenuation can be achieved by cascaded small attenuation units. In this way, millimeter-wave broadband attenuators with good performance can be implemented in the GaAs PHEMT process of a backward node, which provides a way of reducing costs.

4) Capacitive compensation with shunt capacitors connected to the ground both before and after the switch can

be applied in larger attenuation unit designs, particularly in advanced processes, which require fewer cascading units for a larger attenuation range. Notably, a reflective attenuator with compensation of the shunt capacitors connected to the ground both before and after the switch can achieve better performance.

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基于电容补偿技术的毫米波反射式衰减器设计

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摘要:为提升衰减精度和附加相移性能,采用电容补偿技术吸收了开关管的寄生效应,设计了2款5位毫米波反射式衰减器芯片.通过剖析3种基本电容补偿拓扑,借助史密斯圆图,分析负载反射系数、衰减量和附加相移随补偿电容的变化情况,总结出采用电容补偿技术设计反射式衰减器的设计流程和优化方法,并流片验证.2款芯片均集成有1个五位衰减器和1个单刀双掷开关,总芯片面积均为3 mm×1 mm.其中芯片A基于0.5 μm 砷化镓 PHEMT 工艺,采用了尾电容补偿技术;芯片B基于0.15 μm 砷化镓 PHEMT 工艺,采用了开关管前/后电容补偿技术.结果表明,2款芯片包含开关的插入损耗均小于4.5 dB,其中衰减器的插入损耗均小于3 dB,衰减均方根误差都小于0.4 dB,输入1 dB 压缩功率都大于25 dBm,芯片A 衰减相位变动小于±5°,芯片B 衰减相位变动小于±2.5°.

关键词:反射式衰减器;毫米波;容性补偿;低衰减误差;低相位变动

中图分类号:TN454